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## ATS 1992 - 2001 for the first decade

*First Asian Test Symposium, November 26-27, 1992, Hiroshima, Japan*
*Second Asian Test Symposium, November 16-18, 1993, Beijing, China*
*Third Asian Test Symposium, November 15-17, 1994, Nara, Japan*
*Fourth Asian Test Symposium, November 23-24, 1995, Bangalore, India*
*Fifth Asian Test Symposium, November 20-22, 1996, Hsinchu, Taiwan*
*Sixth Asian Test Symposium, November 17-19, 1997, Akita, Japan*
*Seventh Asian Test Symposium, December 2 - 4, 1998, Singapore*
*Eighth Asian Test Symposium, November 16-18, 1999, Shanghai, China*
*Ninth Asian Test Symposium, December 4-6, 2000, Taipei, Taiwan*
*Tenth Asian Test Symposium, November 19-21, 2001, Kyoto, Japan*

**Selected papers in ATS 10th Anniversary Compendium of Papers**

**ATS 1992**
An Approach to Design-for-Testability for Memory Embedded Logic LSIs
 *K.Hatayama, T.Hayashi, M.Takakura, T.Suzuki, S.Michishita, and H.Satoh*
Synthesis for Testability of PLA Based Finite State Machines
 *M.J.Avedillo, J.M.Quintana and J.L.Huertas*
A Concurrent Fault Detection Method for Superscalar Processors
 *A. P. Pawlovsky and M. Hanawa*
A Method of Diagnosing Logical Faults in Combinational Circuits
 *K.Yamazaki and T.Yamada*
Reduction of Dynamic Memory Usage in Concurrent Fault Simulation for
Synchronous Sequential Circuits
 *K.Kim and K.K.Saluja*

**ATS 1993**
Test Set Partitioning and Dynamic Fault Dictionary for Sequential Circuits
 *P.G.Ryan and W.K Fuchs*
A Two-Phase Fault-Simulation Scheme for Sequential Circuits
 *W- C. Wu, C-L.n Lee, and J- E. Chen*
GID--Testable Two-Dimensional Sequential Arrays for Self-Testing
 *W.K.Huang, F.Lombardi, and M.Lu*
A Global BIST Methodology
 *T.Gheewala, H.Sucar, and P.Varma*
On Properties and Implementations of Inverting ALSC for Use in Built-In Self-Testing
 *K Furuya, P.Y.Koh, and E.J.McCluskey*

**ATS 1994**
Efficient Test Sequence Generation for Localization of Multiple Faults in
Communication Protocols
 *Y. Kakuda, H. Yukitomo, S. Kusumoto, and T. Kikuno*
Design of Random Pattern Testable Floating Point Adders
 *J. Rajski and J. Tyszer*
Testability Considerations in Technology Mapping
 *I. Pomeranz and S. M. Reddy*
Analysis and Improvement of Testability Measure Approximation Algorithms
 *J. Bitner, J. Jain, J.A. Abraham, and D.S. Fussell*
Efficiency Improvements for Multiple Fault Diagnosis of Combinational Circuits
 *N. Yanagida, H. Takahashi, and Y. Takamatsu*
Boolean Process - An Analytical Approach to Circuit Representation
 *Y.Min*

**ATS 1995**
Software Transformations for Sequential Test Generation
 *A. Balakrishnan and S. T. Chakradhar*
DC Control and Observation Structures for Analog Circuits
 *Y-R. Shieh and C. W. Wu*

Universal Test Complexity of Field-Programmable Gate Arrays
*T. Inoue, H. Fujiwara, H. Michinishi, T. Yokohira, and T. Okamoto*
A Design-for-Test Technique for Multi-Stage Analog Circuits
*M. Renovell, F. Azais, and Y. Bertrand*
Fanout Fault Analysis for Digital Logic Circuits
*J. E. Chen, C. L. Lee, W. Z. Shen, and B. Chen*
Theory and Applications of Cellular Automata for Synthesis of Easily Testable
Combinational Logic
*S. Nandi and P. Pal Chaudhuri*
Low Power Design and Its Testability
*H. Ueda and K. Kinoshita*

**ATS 1996**
Redundancy Identification Using Transitive Closure
*V.D. Agrawal, M.L. Bushnell, and Q. Lin*
A Consistent Scan Design System for Large-Scale ASICs.
*Y. Konno, K. Nakamura, T. Bitoh, K. Saga, and S. Yano*
Combination of Automatic Test Pattern Generation and Built-In Intermediate Voltage
Sensing for Detecting CMOS Bridging Faults
*K.-J. Lee, J.-J. Tang, T.-C. Huang, and C.-L. Tsai*
Partially Parallel Scan Chain for Test Length Reduction by Using Retiming Technique
*Y. Higami, S. Kajihara, and K. Kinoshita*
An Efficient Compact Test Generator for I$_{DDQ}$ Testing
*H. Kondo and K.-T. Cheng*

**ATS 1997**
FaultMaxx: A Perturbation Based Fault Modeling and Simulation for Mixed-Signal
Circuits
*N. Ben-Hamida, K. Saab, D. Marche, and B. Kaminska*
On the Complexity of Universal Fault Diagnosis for Look-up Table FPGAs
*T. Inoue, S. Miyazaki, and H. Fujiwara*
Testing for the Programming Circuit of LUT-based FPGAs
*H. Michinishi, T. Yokohira, T. Okamoto, T. Inoue, and H. Fujiwara*
Test Length for Random Testing of Sequential Machines Application to RAMs
*R. David*
A Genetic Algorithm for Computation of Initialization Sequences for Synchronous
Sequential Circuits
*F. Corno, P. Prinetto, M. Rebaudengo, M. S. Reorda, and G. Squillero*
On Chip Weighted Random Patterns
*J. Savir*

**ATS 1998**
Vector Restoration Using Accelerated Validation and Refinement.
*S.K. Bommu, S.T. Chakradhar, and K.B. Doreswamy*
March LA: A Test for All Linked Memory Faults
*A.J. van de Goor, G.N. Gaydadjiev, V.N. Yarmolik, and V.G. Mikitjuk*
Test Cycle Count Reduction in a Parallel Scan BIST Environment

*B.Ayari and P. Varma*

BIST TPG for Combinational Cluster (Glue Logic) Interconnect Testing at Board Level
*C.-H. Chiang and S.K. Gupta*

False-Path Removal Using Delay Fault Simulation
*M.A. Gharaybeh, V.D. Agrawal, and M.L. Bushnell*

A Ring Architecture Strategy for BIST Test Pattern Generation
*C. Fagot, O. Gascuel, P. Girard, and C. Landrault*

**ATS 1999**

High Resolution CD-SEM System
*Y. Ose, M. Ezumi, and H. Todokoro*

An Evaluation of Test Generation Algorithms for Combinational Circuits
*S. Xu and T. J. Frank*

An Effective Methodology for Mixed Scan and Reset Design Based on Test Generation and Structure of Sequential Circuits
*H-C. Liang and C. L. Lee*

Circuit Partitioning for Low Power BIST Design with Minimized Peak Power Consumption
*P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch*

New DFT Techniques of Non-Scan Sequential Circuits with Complete Fault Efficiency
*D. K. Das, S. Ohtake, and H. Fujiwara*

**ATS 2000**

Test Generation for Crosstalk-Induced Faults: Framework and Computational Results
*W-Y. Chen, S. Gupta, and M. Breuer*

A Class of Sequential Circuits with Combinational Test Generation Complexity under Single-Fault Assumption
*M. Inoue, E. Gizdarski, and H. Fujiwara*

Fast Hierarchical Test Path Construction for DFT-free Controller-Datapath Circuits
*Y. Makris, J. Collins, and A. Orailoglu*

A New Framework for Static Timing Analysis, Incremental Timing Refinement, and Timing Simulation
*L-C. Chen, S. K. Gupta, and M. A. Breuer*

Accelerated Test Pattern Generators for Mixed-Mode BIST Environments
*W-L. Wang and K-J. Lee*

**ATS 2001**

Short Circuit Faults in State-Of-The-Art ADC's - Are They Hard or Soft?
*A. Lechner, A. M. D. Richardson and B. Hermes*

EB-Testing-Pad Method and its Evaluation by Actual Devices
*N. Kuji and T. Ishihara*

Robust Concurrent Self Test of Linear Digital Systems
*E. Simeu, A. Abdelhay, and M. A. Naal*

Resource Allocation and Test Scheduling for Concurrent Test of Core-Based SOC Design