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ATS 2002 - 2011 for the second decade

Eleventh Asian Test Symposium, November 18-20, 2002, Guam, USA
Twelfth Asian Test Symposium, November 16-19, 2003, Xi'an, China
Thirteenth Asian Test Symposium, November 15-17, 2004, Kenting, Taiwan
Fourteenth Asian Test Symposium, December 18-21, 2005, Kolkata, India
Fifteenth Asian Test Symposium, November 20-23, 2006, Fukuoka, Japan
Sixteenth Asian Test Symposium, October 9-11, 2007, Beijing, China
Seventeenth Asian Test Symposium, November 24-27, 2008, Sapporo, Japan
Eighteenth Asian Test Symposium, November 23-26, 2009, Taichung, Taiwan
Nineteenth Asian Test Symposium, December 1-4, 2010, Shanghai, China
Twentieth Asian Test Symposium, November 21-23, 2011, New Delhi, India

Selected papers in ATS 20th Anniversary Compendium of Papers

ATS 2002

Integrated Test Scheduling, Test Parallelization and TAM Design
Erik Larsson, Klas Arvidsson, Hideo Fujiwara and Zebo Peng

On Generating High Quality Tests for Transition Faults
Yun Shao, Irith Pomeranz and Sudhakar M. Reddy

A Scheduling Method in High-Level Synthesis for Acyclic Partial Scan Design
Tomoo Inoue, Tomokazu Miura, Akio Tamura, and Hideo Fujiwara

Test Scheduling and Test Access Architecture Optimization for System-on-Chips
Huan-Shan Hsu, Jing-Reng Huang, Kuo-Liang Cheng, Chih-Wea Wang

Test Scheduling of BISTed Memory Cores for SOC
Chih-Wea Wang, Jing-Reng Huang, Yen-Fu Lin, Kuo-Liang Cheng, Chih-Tsun Huang, and Chen-Wen Wu

A Concurrent Fault Simulation for Crosstalk Faults in Sequential Circuit
Marong Phadoongsidhi, Kim T. Le, and Kewal K. Saluja

ATS 2003

Test Resource Partitioning Based on Efficient Response Compaction for Test Time and Tester Channels Reduction
Yinhe Han, Yongjun Xu, Huawei Li, Xiaowei Li and Ashuman Chandra

Optimal Scan Tree Construction with Test Vector Modification for Test Compression
Kohei Miyase and Seiji Kajihara

A Processor-Based Built-In Self-Repair Design for Embedded Memories
Chin-Lung. Su, Rei-Fu Huang, andCheng-Wen Wu

Test Synthesis for Datapaths Using Datapath-Controller Functions
Michiko Inoue, Kazuhiro Suzuki, Hiroyuki Okamoto, and Hideo Fujiwara

Test Data Manipulation Techniques for Energy-Frugal, Rapid Scan Test
Ozgur Sinanoglu and Alex Orailoglu

Efficient Diagnosis for Multiple Intermittent Scan Chain Hold-Time Faults
Yu Huang, Wu-Tung Cheng, Cheng-Ju Hsieh, Huan-Yung Tseng, Alou Huang, and Yu-Ting Hung

ATS 2004

Compactor Independent Direct Diagnosis
Wu-Tung Cheng, Kun-Han Tsai, Yu Huang, Nagesh Tamarapalli, and Janusz Rajski

Test Power Reduction with Multiple Capture Orders
Kuen-Jong Lee, Shaing-Jer Hsu, and Chia-Ming Ho

Testing for Missing-Gate Faults in Reversible Circuits
John P. Hayes, Ilia Polian, and Bernd Becker

Intelligible test techniques to support error-tolerance
Melvin Breuer

Multiple Scan Tree Design with Test Vector Modification
Kohei Miyase, Seiji Kajihara, and Sudhakar M. Reddy

High Level Fault Injection for Attack Simulation in Smart Cards
K. Rothbart, U. Neffe, C. Steger, R. Weiss, E. Rieger, and A. Mühlberger

ATS 2005

Untestable multi-cycle path delay faults in industrial designs
Manan Syal, Michael S. Hsiao, Surlyaprakash Natarajan, and Sreejit Chakravarty

A DFT method for RTL data paths based on partially strong testability to guarantee complete fault efficiency
Hiroyuki Iwata, Tomokazu Yoneda, Satoshi Ohtake, and Hideo Fujiwara

Shannon expansion based supply-gated logic for improved power and testability
S. Ghosh, S. Bhunia, and K. Roy

Robust built-in test of RF ICs using envelope detectors
Donghoon Han and Abhijit Chatterjee

Bridge defect diagnosis with physical information
Wei Zou,Wu-Tung Cheng, and Sudhakar M. Reddy

Chip identification using the characteristic dispersion of transistor
Junichi Hirase and Tatsuya Furukawa

ATS 2006

Timing-Aware ATPG for High Quality At-speed Testing of Small Delay Defects
Xijiang Lin, Kun-Han Tsai, Chen Wang, Mark Kassab, Janusz Rajski, Takeo Kobayashi, Randy Klingenberg, Yasuo Sato, Shuji Hamada, and Takashi Aikyo

Interconnect Open Defect Diagnosis with Physical Information
Wei Zou, Wu-Tung Cheng, and Sudhakar Reddy

A Scan Chain Adjustment Technology for Test Power Reduction
Jia Li, Yu Hu, and Xiaowei Li

Power-Aware Test Data Compression for Embedded IP Cores
Nabil Badereddine, Zhanglei Wang, Patrick Girard, Krishnendu Chakrabarty, Arnaud Virazel, Serge Pravossoudovitch, and Christian Landrault

An External Test Approach for Network-on-a-Chip Switches
Jaan Raik, Vineeth Govind, and Raimund Ubar

An Efficient Test Pattern Selection Method for Improving Defect Coverage with Reduced Test Data Volume and Test Application Time
Zhanglei Wang and Krishnendu Chakrabarty

ATS 2007

An Accurate Jitter Estimation Technique for Efficient High Speed I/O Testing
Dongwoo Hong and Kwang-Ting (Tim) Cheng

An On-Chip Test Clock Control Scheme for Multi-Clock At-Speed Testing
Xiao-Xin Fan, Yu Hu, and Laung-Terng (L. -T.). Wang

Improving Test Pattern Compactness in SAT-Based ATPG
Stephan Eggersglub and Rolf Drechsler

Improving Circuit Robustness with Cost-Effective Soft-Error-Tolerant Sequential Elements
Mingjing Chen and Alex Orailoglu

Flip-flop Selection to Maximize TDF Coverage with Partial Enhanced Scan
Gefu Xu, Adit D. Singh

Clues for Modeling and Diagnosing Open Faults with Considering Adjacent Lines
Hiroshi Takahashi, Yoshinobu Higami, Shuhei Kadoyama, Takashi Aikyo, and Yuzo Takamatsu

ATS 2008

Test Power Reduction by Blocking Scan Cell Outputs
Xijiang Lin and Janusz Rajski

Low-Cost One-Port Approach for Testing Integrated RF Substrates
Abhilash Goyal and Madhavan Swaminathan

Interconnect-Driven Layout-Aware Multiple Scan Tree Synthesis for Test Time, Data Compression and Routing Optimization
Katherine Shu-Min Li, and Jr-Yang Huang

Untestable Fault Identification in Sequential Circuits Using Model-Checking
Jaan Raik, Hideo Fujiwara, Raimund Ubar, and Anna Krivenko

A Test Generation Method for State-Observable FSMs to Increase Defect Coverage under the Test Length Constraint
Ryoichi Inoue, Toshinori Hosokawa, and Hideo Fujiwara

A Re-design Technique of Datapath Modules in Error Tolerant Application
Doochul Shin and Sandeep K. Gupta

ATS 2009

A Non-intrusive and Accurate Inspection Method for Segment Delay Variabilities
Ying-Yen Chen and Jing-Jia Liou

CAT: A Critical-Area-Targeted Test Set Modification Scheme for Reducing Launch Switching Activity in At-Speed Scan Testing
K. Enokimoto, X. Wen, Y. Yamato, K. Miyase, H. Sone, S. Kajihara, M. Aso, and H. Furukawa

BIST Driven Power Conscious Post-Manufacture Tuning of Wireless Transceiver Systems Using Hardware-Iterated Gradient Search
Vishwanath Natarajan, Shyam Kumar Devarakond, Shreyas Sen, and Abhijit Chatterjee

A Practical Approach to Threshold Test Generation for Error Tolerant Circuits
Hideyuki Ichihara, Kenta Sutoh, Yuki Yoshikawa, and Tomoo Inoue

M-IVC: Using Multiple Input Vectors to Minimize Aging-induced Delay
Song Jin, Yinhe Han, Lei Zhang, Huawei Li, Xiaowei Li, and Guihai Yan

An On-Chip Integrator Leakage Characterization Technique and Its Application to Switched Capacitor Circuits Testing
Chen-Yuan Yang, Xuan-Lun Huang, and Jiun-Lang Huang

ATS 2010

Tackling the Path Explosion Problem in Symbolic Execution-driven Test Generation
Saparya Krishnamoorthy, Michael Hsiao, and Loganathan Lingappan

Rapid Radio Frequency Amplitude and Phase Distortion Measurement Using Single-tone AM Stimulus
Shreyas Sen, Shyam Devarakond, and Abhijit Chatterjee

Variation-Aware Fault Modeling
Fabian Hopsch, Bernd Becker, Sybille Hellebrand, Ilia Polian, Bernd Straube

Diagnosis of Multiple Physical Defects Using Logic Fault Models
Xun Tang, Wu-Tung Cheng, Ruifeng Guo, and Sudhakar Reddy
Power-Safe Application of Transition Delay Fault Patterns Considering Current Limit during Wafer Test
Wei Zhao, Junxia Ma, Mohammad Tehranipoor, and Sreejit Chakravarty
Circuit Topology-Based Test Pattern Generation for Small-Delay Defects
Sandeep Kumar Goel, Krishnendu Chakrabarty, Mahmut Yilmaz, Ke Peng, and Mohammad Tehranipoor

ATS 2011
Improving the accuracy of RF alternate test using multi-VDD conditions: application to envelope-based test of LNAs
Manuel J. Barragan, Rafaella Fiorelli, Gildas Leger, Adoracion Rueda and Jose Luis Huertas
Fault Diagnosis in Memory BIST Environment with Non-March Tests
Jerzy Tyszer, Grzegorz Mrugalski, Artur Pogiel, Nilanjan Mukherjee, Janusz Rajski and Pawel Urbanek
Diagnosing Multiple Slow Gates for Performance Tuning in the face of Extreme Process Variations
Xi Qian, Adit Singh and Abhijit Chatterjee
Post-Silicon Timing Validation Method using Path Delay Measurements
Eun Jung Jang, Jaeyong Chung, Anne Gattiker, Sani Nassif and Jacob Abraham
An Efficient 2-Phase Strategy to Achieve High Branch Coverage
Sarvesh Prabhu, Michael Hsiao, Saparya Krishnamoorthy, Loganathan Lingappan, Vijay Gangaram and Jim Grundy
Efficient BDD-based Fault Simulation in Presence of Unknown Values
Michael Kochte, Sandip Kundu, Kohei Miyase, Xiaoqing Wen and H.-J. Wunderlich
Characterizing Pattern Dependent Delay Effects in DDR Memory Interfaces
Atul Gupta, Ajay Kumar and Manas Chhabra