ATS 2010
Advance Technical Program

(Hotel Four Points by Sheraton, Daning, Shanghai, December 1 – 4, 2010)

Dec. 01, 2010		
Registration (9:00-20:30) and Tutorial (13:00-17:30)		
Dec. 02, 2010		
Session 1: Opening Session **Session Chair:** **Dec. 02, 8: 45 – 9: 30**		
Session 2: Plenary Session (Keynote Speech) **Session Chair:** **Dec. 02, 9:50 – 11:50**		
1	**Title**	**Keynote Speech** (1)
	Speaker	**To be decided soon**
2	**Title**	**Keynote Speech** (2)
	Speaker	**To be decided soon**
Session 3A: Analog & Mixed-Signal testing / RF/ High Speed I/O Testing **Session Chair:** **Dec. 02, 13:00-15:00**		
1	**Title**	Rapid Radio Frequency Amplitude and Phase Distortion Measurement Using Single Sine wave Modulated RF Stimulus
	Authors	*Shreyas Sen, Shyam Devarakond and Abhijit Chatterjee*
2	**Title**	Digitally Assisted Concurrent Built-In Tuning of RF Systems Using Hamming Distance Proportional Signatures
	Authors	*Shyam Kumar Devarakond, Shreyas Sen, Vishwanath Natarajan, Aritra Banerjee, Hyun Choi, Ganesh Srinivasan and Abhijt Chatterjee*
3	**Title**	The Test Ability of an Adaptive Pulse Wave for ADC Testing
	Authors	*Xiaoqin Sheng and Hans Kerkhoff*
4	**Title**	Bayesian Fault Diagnosis of RF Circuits Using Nonparametric Density Estimation
	Authors	*Ke Huang, Haralampos-G. Stratigopoulos and Salvador Mir*

Session 3B: System-on-a-Chip Test / System-in-Package Test **Session Chair:** **Dec. 02, 13:00-15:00**		
1	**Title**	A Test Integration Methodology for 3D Integrated Circuits
	Authors	*Che-Wei Chou, Jin-Fu Li, Ji-Jan Chen, Ding-Ming Kwai, Yung-Fa Chou and Cheng-Wen Wu*
2	**Title**	Application-Aware Online Testing for Many-Core SoC
	Authors	*Jason Lee, Suman Mandal and Rabi Mahapatra*
3	**Title**	Performance Characterization of TSV in 3D IC via Sensitivity Analysis
	Authors	*Jhih-wei You, Shi-Yu Huang, Ding-Ming Kwai, Yung-Fa Chou and Cheng-Wen Wu*
4	**Title**	Temperature-Aware SoC Test Scheduling Considering Inter-Chip Process Variation
	Authors	*Nima Aghaee, Zhiyuan He, Zebo Peng and Petru Eles*
Session 3C: Special Session for Doctoral Contest **Session Chair:** **Dec. 02, 13:00-15:00**		
	Title	Reports will be delivered in this Session
	Contester	See detail information of Doctoral Contest
Session 4A: Automatic Test Equipment & Memory and FPGA Testing **Session Chair:** **Dec. 02, 15:20-17:20**		
1	**Title**	At-speed Test of High-speed DUT using Built-off Test Interface
	Authors	*Joonsung Park, Jae Wook Lee, Jaeyong Chung, Kihyuk Han, Jacob Abraham, Eonjo Byun, Cheol-Jong Woo and Sejang Oh*
2	**Title**	Particle Swarm Optimization Based Scheme for Low Power March Sequence Generation for Memory Testing
	Authors	*Krishna Kumar S, S. Kaundinya and Santanu Chattopadhyay*
3	**Title**	New Microcode's Generation Technique for Programmable Memory Built-In Self Test
	Authors	*Nur Qamarina Mohd Noor, Azilah Saparon, Yusrina Yusof and Mahmud Adnan*
4	**Title**	*A Smart RTL Verification System for Internal Signal Probing and Behavior Trace
	Authors	*Yu-lin Wang, Chung-Ping Young and Alvin W.Y. Su*

Session 4B: Low Power Testing **Session Chair:** **Dec. 02, 15:20-17:20**		
1	**Title**	Adaptive Low Shift Power Test Pattern Generator for Logic BIST
	Authors	*Xijiang Lin and Janusz Rajski*
2	**Title**	Power Supply Noise Reduction in Broadcast-Based Compression Environment for At-Speed Scan Testing
	Authors	*Chun-Yong Liang, Meng-Fan Wu and Jiun-Lang Huang*
3	**Title**	Modified Scan Flip-Flop for Low Power Testing
	Authors	*Amit Mishra, Nidhi Sinha, Satdev, Virendra Singh, Sreejit Chakravarty and Adit Singh*
4	**Title**	Capture in Turn Scan for Reduction of Test Data Volume, Test Application Time and Test Power
	Authors	*Zhiqiang You, Jiedi Huang, Michiko Inoue, Jishun Kuang and Hideo Fujiwara*
Session 4C: Software Testing and Reliability Model **Session Chair:** **Dec. 02, 15:20-17:20**		
1	**Title**	Tackling the Path Explosion Problem in Symbolic Execution-driven Test Generation for Programs
	Authors	*Saparya Krishnamoorthy, Michael Hsiao and Loganathan Lingappan*
2	**Title**	A Reliability Model for Object-Oriented Software
	Authors	*Peng Xu and Shiyi Xu*
3	**Title**	A New Approach to Generating High Quality Test Cases
	Authors	*Pan Liu and Huaikou Miao*
4	**Title**	A Study on Software Reliability Prediction Based on Transduction Inference
	Authors	*Jun-Gang Lou, Jian-Hui Jiang, Chun-Yan Shuai and Ying Wu*
Dec. 03, 2010		
Session 5A: Board and System Testing / On-line Testing **Session Chair:** **Dec. 03, 08:30-10:00**		
1	**Title**	Software-Based Self-Testing of Processors Using Expanded Instructions
	Authors	*Ying zhang, Huawei Li and Xiaowei Li*

2	**Title**	Mimicking of Functional State Space with Structural Tests for the Diagnosis of Board-Level Functional Failures
	Authors	*Hongxia Fang, Zhiyuan Wang, Xinli Gu and Krishnendu Chakrabarty*
3	**Title**	Optimization and Selection of Diagnosis-Oriented Fault-Insertion Points for System Test
	Authors	*Zhaobo Zhang, Zhanglei Wang, Xinli Gu and Krishnendu Chakrabarty*
Session 5B: Test Generation & Fault Simulation (1) **Session Chair:** **Dec. 03, 08:30-10:00**		
1	**Title**	Efficient Simulation of Structural Faults for the System Reliability Evaluation at System Level
	Authors	*Michael Kochte, Christian Zoellin, Rafal Baranowski, Michael Imhof, Hans-Joachim Wunderlich, Nadereh Hatami, Stefano Di Carlo and Paolo Prinetto*
2	**Title**	Jitter Characterization of Pseudo-Random Bit Sequences Using Incoherently Sub-Sampling
	Authors	*Hyun Choi and Abhijit Chatterjee*
3	**Title**	On Selection of Testable Paths with Specified Lengths for Faster-Than-At-Speed Testing
	Authors	*Xiang Fu, Huawei Li and Xiaowei LI*
Session 5C: Failure Analysis / Fault Modeling (1) **Session Chair:** **Dec. 03, 08:30-10:00**		
1	**Title**	Variation-Aware Fault Modeling
	Authors	*Fabian Hopsch, Bernd Becker, Sybille Hellebrand, Ilia Polian, Bernd Straube, Wolfgang Vermeiren and Hans-Joachim Wunderlich*
2	**Title**	Diagnosis of Multiple Physical Defects Using Logic Fault Models
	Authors	*Xun Tang, Wu-Tung Cheng, Ruifeng Guo and Sudhakar Reddy*
3	**Title**	A Memory Fault Simulator for Radiation-Induced Effects in SRAMs
	Authors	*Paolo Rech, Alberto Bosio, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel and L. Dilillo*
Session 6A: Built-in Self-Test / Embedded Testing (1) **Session Chair:** **Dec. 03, 10:20-12:00**		
1	**Title**	A Low Cost Built-In Self-Test Circuit for High-Speed Source Synchronous Memory Interfaces
	Authors	*Hyunjin Kim and Jacob A. Abraham*

2	**Title**	A Complete Logic BIST Technology with No Storage Requirement
	Authors	*Wei-Cheng Lien and Kuen-Jong Lee*
3	**Title**	Efficient embedding of deterministic test data
	Authors	*Mudassar Majeed, Daniel Ahlström, Urban Ingelsson, Gunnar Carlsson and Erik Larsson*
Session 6B: Test Generation & Fault Simulation (2) **Session Chair:** **Dec. 03, 10:20-12:00**		
1	**Title**	FSimGP²: An Efficient Fault Simulator with GPGPU
	Authors	*Min Li and Michael Hsiao*
2	**Title**	A Quasi-Best Random Testing
	Authors	*Shiyi Xu and Peng Xu*
3	**Title**	Design of DSP virtual machine oriented all-digital simulation and testing
	Authors	*Chongwen Wang and Gangyi Ding*
4	**Title**	Formula-Oriented Compositional Minimization in Model Checking
	Authors	*Bowen Chen, Haihua Shen and Wenhui Zhang*
Session 6C: Failure Analysis / Fault Modeling (2) **Session Chair:** **Dec. 03, 10:20-12:00**		
1	**Title**	On Soft Error Immunity of Sequential Circuits
	Authors	*Dan Zhu, Tun Li and SiKun Li*
2	**Title**	Testing of Digital Microfluidic Biochips using Improved Eulerization Techniques and the Chinese Postman Problem
	Authors	*Debasis Mitra, Sarmishtha Ghoshal, Hafizur Rahaman, Krishnendu Chakrabarty and Bhargab B Bhattacharya.*
3	**Title**	P²CLRAF: An Pre- and Post-silicon Cooperated Circuit Lifetime Reliability Analysis Framework
	Authors	*Song Jin, Yinhe Han, Huawei Li and Xiaowei Li*

Afternoon Tour in Shanghai **(13:00 — 18:00)**		
Night Banquet **(18:30 — 21:00)**		
Dec. 04, 2010		
Session 7A: Built-in Self-Test / Embedded Testing (2) **Session Chair:** **Dec. 04, 08:30-10:00**		
1	**Title**	Built-in Self-Test for Capacitive MEMS using a Charge Control Technique
	Authors	*Iftekhar Ibne Basith, Nabeeh Kandalaft and Rashid Rashidzadeh*
2	**Title**	Defect Coverage-Driven Window-Based Test Compression
	Authors	*Xrysovalantis Kavousianos, Krishnendu Chakrabarty, Emmanouil Kalligeros and Vasileios Tenentes*
3	**Title**	Test Data Reduction for BIST-aided Scan Test Using Compatible Flip-flops and Shifting Inverter Code
	Authors	*Masashi Ishikawa, Hiroyuki Yotsuyanagi and Masaki Hashizume*
Session 7B: Test Generation & Fault Simulation (3) **Session Chair:** **Dec. 04, 08:30-10:00**		
1	**Title**	Testing of Low-Cost Digital Microfluidic Biochips with Non-Regular Array Layouts
	Authors	*Yang Zhao and Krishnendu Chakrabarty*
2	**Title**	Derivation of Optimal Test Set for Detection of Multiple Missing-Gate Faults in Reversible Circuits
	Authors	*Dipak K. Kole, Hafizur Rahaman, Debesh K Das and Bhargab B. Bhattacharya*
3	**Title**	On Determining the Real Output Xs by SAT-Based Reasoning
	Authors	*Melanie Elm, Michael Kochte and Hans-Joachim Wunderlich*
4	**Title**	* Test Pattern Selection and Compaction for Sequential Circuits in an HDL Environment
	Authors	*Mohammad Hashem Haghbayan, Sara Karamati, Fatemeh Javaheri and Zanalabedin Navabi*

Session 7C: DFX: Design for Testability, Reliability, Dependability… (1) **Session Chair:** **Dec. 04, 08:30-10:00**		
1	**Title**	Pattern Encodability Enhancements for Test Stimulus Decompressors
	Authors	*Nader Alawadhi, Ozgur Sinanoglu and Mohammed Al-Mulla*
2	**Title**	High Performance Compaction for Test Responses with Many Unknowns
	Authors	*Thomas Rabenalt, Michael Richter and Michael Goessel*
3	**Title**	Design-for-Test of Digitally-Assisted Analog IPs for Automotive SoCs
	Authors	*Yizi Xing and Liquan Fang*
Session 8A: Built-in Self-Test / Embedded Testing (3) **Session Chair:** **Dec. 04, 10:20-12:00**		
1	**Title**	Controlling Peak Power Consumption for Scan Based Multiple Weighted Random BIST
	Authors	*Hiroshi Yokoyama, Hideo Tamamoto and Kewal K. Saluja*
2	**Title**	Parallel LFSR Reseeding With Selection Register For Mixed-Mode BIST
	Authors	*Piyanart Kongtim and Taweesak Reungpeerakul*
3	**Title**	On-chip Jitter Measurement Using Vernier Ring Time-to-digital Converter
	Authors	*Jianjun Yu and Fa Dai*
Session 8B: Yield Enhancement / Silicon Debug (1) **Session Chair:** **Dec. 04, 10:20-12:00**		
1	**Title**	HYPERA: High-Yield Performance-Efficient Redundancy Analysis
	Authors	*Tsung-Chu Huang, Kuei-Yeh Lu and Yen-Chieh Huang*
2	**Title**	A Comprehensive System-on-Chip Logic Diagnosis
	Authors	*Youssef Benabboud, Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel and Olivia Riewer*

3	**Title**	On Signal Tracing for Debugging Speedpath-Related Electrical Errors in Post-Silicon Validation
	Authors	*Xiao Liu and Qiang Xu*
Session 8C: DFX: Design for Testability, Reliability, Dependability…(2) **Session Chair:** **Dec. 04, 10:20-12:00**		
1	**Title**	Substantial Fault Pair at A Time (SFPAT): An Automatic Diagnostic Pattern Generation Method
	Authors	*Jing Ye, Xiaolin Zhang, Yu Hu and Xiaowei Li*
2	**Title**	D-Scale: A Scalable System-level Dependable Method for MPSoCs
	Authors	*Nicolas Hebert, Pascal Benoit, Gilles Sassatelli and Lionel Torres*
3	**Title**	Bipartite Full Scan Design: A DFT Method for Asynchronous Circuits
	Authors	*Hiroshi Iwata, Satoshi Ohtake, Michiko Inoue and Hideo Fujiwara*
Session 9A: Delay Fault Testing (1) **Session Chair:** **Dec. 04, 13:00-14:50**		
1	**Title**	Power-Safe Application of Transition Delay Fault Patterns Considering Current Limit during Wafer Test
	Authors	*Wei Zhao, Junxia Ma, Mohammad Tehranipoor and Sreejit Chakravarty*
2	**Title**	Circuit Topology-Based Test Pattern Generation for Small-Delay Defects
	Authors	*Sandeep Kumar Goel, Krishnendu Chakrabarty, Mahmut Yilmaz, Ke Peng and Mohammad Tehranipoor*
3	**Title**	Seed Ordering and Selection for High Quality Delay Test
	Authors	*Tomokazu Yoneda, Michiko Inoue, Akira Taketani and Hideo Fujiwara*
4	**Title**	On Bias in Transition Coverage of Test Sets for Path Delay Faults
	Authors	*Irith Pomeranz and Sudhakar Reddy*

Session 9B: Yield Enhancement / Silicon Debug (2) **Session Chair:** **Dec. 04, 13:00-14:50**		
1	**Title**	HYPER: A Heuristic for Yield/Area Maximizing Improvement using Redundancy in SoC
	Authors	*Mohammad Mirza-Aghatabar, Melvin Breuer and Sandeep Gupta*
2	**Title**	Enhance Profiling-Based Scan Chain Diagnosis by Pattern Masking
	Authors	*Wu-Tung Cheng and Yu Huang*
3	**Title**	Maximal Resilience for Reliability and Yield Enhancement in Interconnect Structure
	Authors	*Chih-Yun Pai and Shu-Min Li*
Session 9C: DFX: Design for Testability, Reliability, and Dependability… (3) **Session Chair:** **Dec. 04, 13:00-14:50**		
1	**Title**	XOR-Based Response Compactor Adaptive to X-Density Variation
	Authors	*Samah Saeed and Ozgur Sinanoglu*
2	**Title**	DFT + DFD: An Integrated Method for Design for Testability and Diagnosability
	Authors	*Nikhil Rahagude, Maheshwar Chandrasekar and Michael Hsiao*
3	**Title**	Thermal Safe High Level Test Synthesis for Hierarchical Testability
	Authors	*Tung-Hua Yeh and Sying-Jyan Wang*
4	**Title**	Accelerating Strategy for Functional Test of NoC Communication Fabric
	Authors	*Yan Zheng, Hong Wang, Shiyuan Yang, Chen Jiang and Feiyu Gao*
Session 10A: Delay Fault Testing (2) **Session Chair:** **Dec. 04, 15:10-17:10**		
1	**Title**	An Efficient Algorithm for Finding a Universal Set of Testable Long Paths
	Authors	*Zijian He, Tao Lv, Huawei Li and Xiaowei Li*
2	**Title**	Distinguishing Resistive Small Delay Defects from Random Parameter Variations
	Authors	*Xi Qian and Adit D. Singh*

3	**Title**	A Low Area On-Chip Delay Measurement System Using Embedded Delay Measurement Circuit
	Authors	*Kentaroh Katoh, Kazuteru Namba and Hideo Ito*
4	**Title**	A Noise-Aware Hybrid Method for SDD Pattern Grading and Selection
	Authors	*Ke Peng, Mahmut Yilmaz, Krishnendu Chakrabarty and Mohammad Tehranipoor*
Session 10B: Test Economics / Functional Verification / Failure Analysis **Session Chair:** **Dec. 04, 15:10-17:10**		
1	**Title**	Test Cost Analysis for 3D Die-to-Wafer Stacking
	Authors	*Mottaqiallah Taouil, Said Hamdioui, Kees Beenakker and Erik Jan Marinissen*
2	**Title**	Mining Complex Boolean Expressions for Sequential Equivalence Checking
	Authors	*Neha Goel, Michael Hsiao, Naren Ramakrishnan and Mohammed Zaki*
3	**Title**	On-the-fly Reduction of Stimuli for Functional Verification
	Authors	*Qi Guo, Tianshi Chen, Haihua Shen, Yunji Chen and Weiwu Hu*
4	**Title**	Test Time Analysis for IEEE P1687
	Authors	*Farrokh Ghani Zadegan, Urban Ingelsson, Gunnar Carlsson and Erik Larsson*

- The Advance Program is subject to change without notice until a Final Program is released.
- Papers with an asterisk "*" had not been submitted to IEEE CPS before Sept. 9, 2010.