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Call For Papers ATS'12

The 21st Asian Test Symposium

November 19-22, 2012, Toki Messe Niigata Convention Center, Niigata, Japan

SCOPE

The Asian Test Symposium (ATS) provides an international forum for engineers and researchers from all countries of the world, especially from Asia, to present and discuss various aspects of device, board and system testing with design, manufacturing and field considerations in mind.

Major topics include, but are not limited to:

- Automatic Test Pattern Generation (ATPG)
- Analog Test / Mixed-Signal Test •
- Boundary Scan Test .
- Board and System Test .
- .
- Design for Testability (DFT) .
- Design Verification and Validation
- Defect-Based Testing
- Delay and Performance Test
- Diagnosis and Debug

SUBMISSIONS

- Fault Modeling and Simulation
- Fault Tolerance
- High-Speed I/O Test / RF Testing
- Memory Test / FPGA Test
- **On-Line** Test
- System-on-a-Chip Test
- System-in-package (SiP)/ 3D Test
- Software Testing / Software Design for Testing
- Test Compression
- Temperature/Power-aware Test
- Test Quality
- Yield Analysis and Enhancement

Regular Session: The ATS'12 Program Committee invites original, unpublished paper submissions for ATS'12. A submission will be considered as evidence that, upon acceptance, the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication.

Industry Session: This session will address a wide range of practical problems in LSI test, board and system test, diagnosis, failure analysis, design verification, and so on. The session will consist of poster presentations and optional oral presentations. A one-page abstract is required for submission. Each submission should also include the complete address and designate a contact person and a presenter. Abstract submissions should be emailed to Industry Chair (ats12-industry@aries30.cse.kyutech.ac.jp).

Doctoral Thesis Award: The Award serves the purpose to promote most impactful doctoral student work, to provide the students with the exposure to the community and the prospective employers, and to support interaction between academia and industry in the field of test technology. This major Award is named after Prof. Edward J. McCluskey, a key educator and mentor in the fields of test technology, logic design, and reliability. Call for paper of this award is available on the ATS2012 website (http://aries3a.cse.kyutech.ac.jp/~ats12/).

KEY DATES (Regular Session)

Submission deadline: June 15, 2012 (Submission site has been already closed.) Notification of acceptance: Aug. 5, 2012 Camera ready manuscript: Aug. 31, 2012

KEY DATES (Industry Session) Submission deadline: Jul. 19, 2012 Notification of acceptance: Aug. 5, 2012 Camera ready manuscript: Aug. 31, 2012

KEY DATES (Dr. Thesis Award)

Submission deadline: Aug. 20, 2012 Notification of acceptance: Sep. 20, 2012



For general information General Chair: Kazumi Hatayama (ats12-gc@aries30.cse.kyutech.ac.jp)

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ATS2012 WEBSITE http://aries3a.cse.kyutech.ac.jp/~ats12/

- **Built-In Self-Test**

 - Dependable System
 - Economics of Test