ATS'14

November 16-19, 2014. Hangzhou, China

The 23rd Asian Test Symposium

NEWS

2014/11/06	**On-site Registration**
2014/08/26	Registration System online.
2014/08/09	Accepted Papers.
2014/05/07	ATS Doctoral Thesis Award.
2014/05/04	Submission system is opened.
2014/04/24	ATS Best Paper Award.

Important Deadlines

Submission deadline:	~~May. 23,2014~~
Notification of acceptance:	~~Aug. 10, 2014~~
Camera ready manuscript:	~~Sept. 05, 2014~~

Sponsors

IEEE Computer Society

Test Technology Technical Council

Institute of Computing Technology

Best Paper Award: ATS'14 will present a Best Paper Award to a selected paper of exceptional quality. The evaluation will be conducted by an award committee constituted by experts covering all aspects of test technology, based on the criteria of innovation, potential impact, and presentation quality.

Diamond Supporter:

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It's recommended that you access this website using IE7 or Firefox

Conference Admin

ATS'14

November 16-19, 2014. Hangzhou, China

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Symposium Overview

The Asian Test Symposium (ATS) provides an open forum for researchers and industrial practitioners from all countries of the world, especially from Asia, to exchange innovative ideas on system, board, and device testing with design, manufacturing and field consideration in mind.

Original papers on, but not limited to, the following areas are invited.

- Automatic Test Pattern Generation
- Fault Modeling and Simulation
- Design Verification and Validation
- Diagnosis and Debug
- Board and System Test
- Analog/Mixed-Signal Test
- High-Speed I/O Test
- RF Test
- Delay and Performance Test
- Memory Test/FPGA Test
- System-in-Package/3D Test
- Software Testing
- Boundary Scan Test
- Built-In Self-Test
- Design-for-Testability
- Test Compression
- On-Line Test
- Temperature/Power-Aware Testing
- Defect-Based Testing
- Fault Tolerance
- Dependable System
- Yield Analysis and Enhancement
- Test Quality
- Economics of Test
- Hardware Security

Submissions

Regular Sessions: The ATS'14 Program Committee invites original, unpublished paper submissions on the above topics. Paper submissions should be complete manuscripts, not exceeding six pages (including figures, tables, and bibliography) in a standard IEEE two-column format. The submission will be considered evidence that upon acceptance the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication.

ATS'14 will present a Best Paper Award to a selected paper of exceptional quality. The evaluation will be conducted by an award committee constituted by experts covering all aspects of test technology, based on the criteria of innovation, potential impact, and presentation quality.

Key Dates

• Submission deadline:	~~May 16, 2014~~ May 23,2014(extended)
• Notification of acceptance:	Aug. 10, 2014
• Camera ready manuscript:	Sept. 5, 2014

Further Information

Email: ats14@ict.ac.cn

URL: http://ats2014.ict.ac.cn

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News

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2014/08/09	Accepted Papers
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2014/05/07	ATS Doctoral Thesis Award.
2014/05/04	Submission System is Opened!

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- **General Co-Chair(s)**

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2005-2006: Cheng-Wen Wu, National Tsing Hua University, Taiwan
2007-2010: Seiji Kajihara, Kyushu Institute of Technology, Japan
2011-2013: Xiaowei Li, Chinese Academy of Sciences, China

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- WRTLT'14
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Contact Us

Please feel free to contact us if you have any question. Thank you.

Conference Program Chair: Yinhe Han

Email: yinhes@ict.ac.cn

Conference Web Chair: Long Tian

Email: tianlong@ict.ac.cn

Tel:(010)62600718

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Date & Location

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VISA

- Visas are needed for most non-Chinese nationals to enter China (exceptions are passport holders from Singapore, Brunei, and Japan). Application should be made to the Chinese Embassy/Consulate in your country of residence. There are two types of visas, Tourist Visa (**L Visa**) and Business Visa (**F Visa**).

- For a Tourist Visa, you should check with the Chinese Embassy/Consulate in your country of residency to determine the local rules that apply for your tourist visa application. You may need to show evidence of bookings for your return flights and hotel. For most countries, a Tourist Visa does not require an official invitation letter.

- In China, invitation letters are issued by the Ministry of Foreign Affairs. We need about one month to apply it after we receive your request. Therefore, we strongly recommend you to apply for the Tourist Visa. If an invitation letter is still required, please let us know.
- To request an invitation letter, you need first register for the conference and then forward the registration confirmation email, along with your request to ats14@ict.ac.cn.

- Citizens from many countries can enter Hongkong without a visa. For those who do plan to go through Hongkong, please note that you still need a Chinese Visa to enter Shenzhen. If you will travel between Hongkong and Shenzhen multiple times, you need to apply for a multi-entry visa.

- We expect that most attendees can use a Tourist Visa.
- An official invitation letter is required to apply for a Business Visa.
- You can find the website of Chinese Embassy/Consulate in your country from here.

Please feel free to contact us if you have any question about VISA. Thank you.

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Venue

The 2014 ATS will be held in the *Hangzhou Jinxi Hotel*.

Address:
Hangzhou Jinxi Hotel
No.39 Causeway yang ,Hangzhou, China
TEL: (+86)0571-87992288-6901

- To receive the conference discount rate for Hangzhou Jinxi Hotel, please fill and return *this form* via e-mail to *ats14@ict.ac.cn* by **October 15, 2014.**

Conference Transportation

1) Arriving at the Xiaoshan airport

The **map** from Airport of Xiaoshan to Jinxi Hotel.

Upon Arriving at the Xiaoshan airport, we recommend two ways to get to Hangzhou Jinxi Hotel.

- **By airport shuttle bus**: It takes about one hour to take a airport shuttle bus from airport to Hangzhou Railway Station. Take a taix when you get off the bus to Jinxi Hotel.
- **By Taix**: It takes about RMB 120 from airport to Jinxi Hotel.

2) Arriving at the Hangzhoudong Railway Station

The **map** from Hangzhoudong Railway Station to Jinxi Hotel.

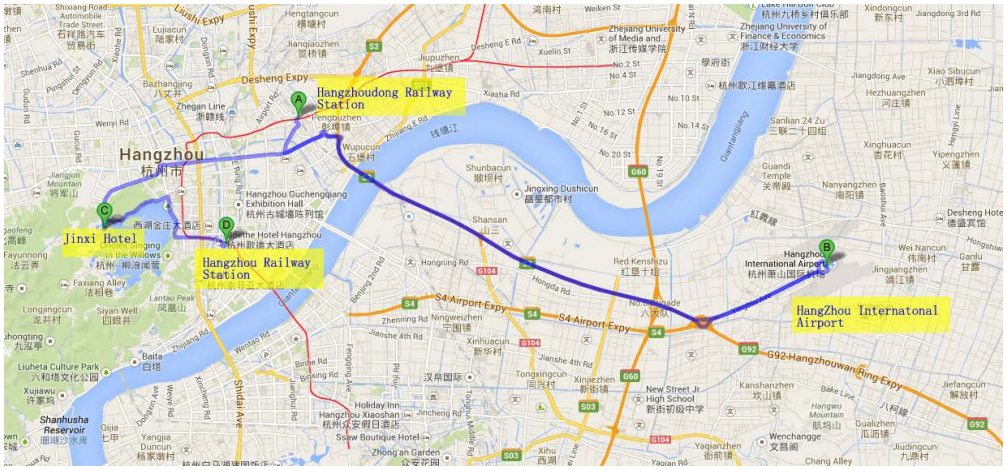
Upon arriving at Hangzhoudong Railway Station, we recommend you take a taxi to Jinxi Hotel.

3) Arriving at the Hangzhou Railway Station

The **map** from Hangzhou Railway Station to Jinxi Hotel.

Upon arriving at Hangzhou Railway Station, we recommend you take a taxi to Jinxi Hotel.

Location



Location A : Hangzhoudong Railway Station (about 12 km to Jinxi Hotel)

Location B: Hangzhou International Airport (Xiaoshan)(about 35 km to Jinxi Hotel)

Location C: Jinxi Hotel

Location D: Hangzhou Railway Station (about 8 km to Jinxi Hotel)

Click here to view large map.

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Accommodation

Hangzhou Jinxi Hotel(杭州金溪山庄)

Address	No.39 Causeway yang, Hangzhou
WWW	http://www.jinxihotel.com/weben/Public/Default.aspx
Reservation	1、Please fill and return the hotel reservation form (doc) by **October 15, 2014** to receive the conference discount rate. (Limited availability.) 2、Reservation by email: ats14@ict.ac.cn.
Direction	Please check "Venue" for details.
Room Rate	View it in JinxiHotel Reservation Form.
Contact	TEL：(+86)0571-87992288-690

Other Hotels:

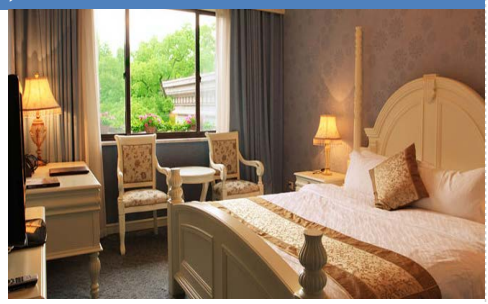
- The conference only offer hotel reservation for the ATS14 venue, Hangzhou Jinxi Hotel.
- If you want to select other hotels, you can refer to the following hotels which are in walking distance to the venue.
- You should contact these hotels by yourself for reservation.
- Room rates in the following tables are just for reference. Please contact the hotel to get the exact rates for reservation.

Lotus Glade Hotel 52(莲遇52度假酒店)

Address	No. 38 Yang Gongdi , Xihu District, Hangzhou
WWW	http://www.lianyu52.com/
Distance To Venue	6 minutes' walk to JinxiHotel. Please view the map below for details.
Room Rate	Garden View Room: RMB 768; Scenery Room RMB 818

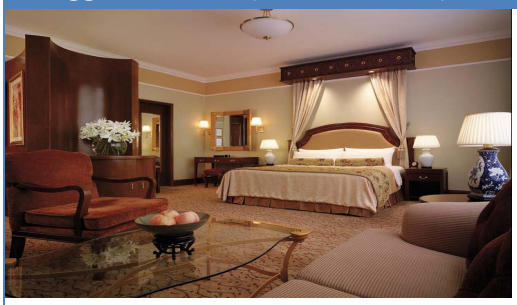
Contact	TEL：(+86)0571-87999767

Hangzhou The New Hotel (杭州新新饭店)

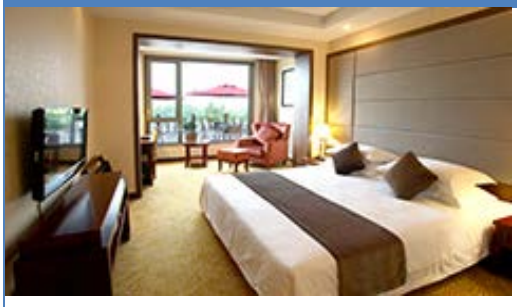
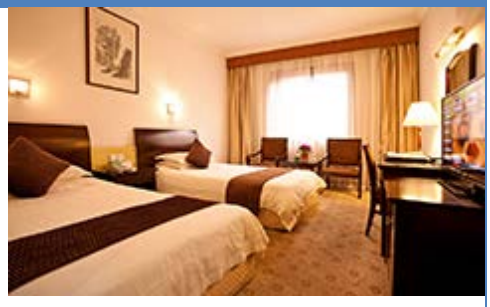
Address	No. 58 North Hill Street, Hangzhou
WWW	http://www.thenewhotel.com/Home/Index?lan=en-us
Distance To Venue	12 minutes' walk to JinxiHotel. Please view the map below for details.
Room Rate	Standard Room: RMB 686; King Room: RMB 868
Contact	TEL：(+86)0571-87660000

Shanggri-La Hotel (香格里拉饭店)




Address	No. 78 Beishan Road, Hangzhou, China
WWW	http://www.shangri-la.com/hangzhou/shangrila/
Distance To Venue	8 minutes' walk to Jinxi Hotel. Please view the map below for details.
Room Rate	Standard Room: RMB 1058
Contact	TEL：(+86)0571-87977951

Huabei Hotel (华北饭店)

Address	No. 18 Qixia Rideg, Hangzhou, China
WWW	http://www.hzhbfd.com/main.asp
Distance To Venue	About 15 minutes' walk to Jinxi Hotel. Please view the map below for details.
Room Rate	Standard Room: RMB 508; Deluxe Standard Room: RMB 628
Contact	TEL：(+86)0571-87977951

Hotels Location :

Location A: Hangzhou The New Hotel

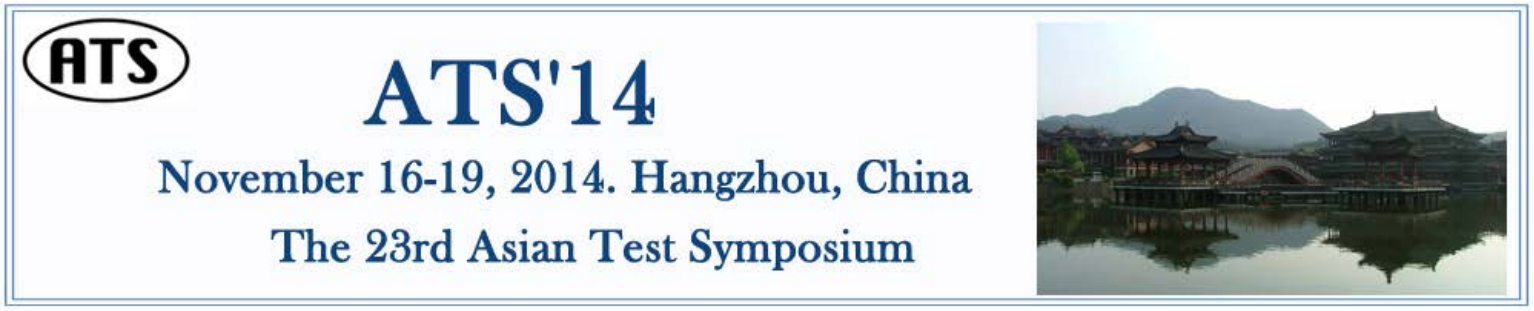
Location B: Shanggri-La Hotel

Location C: Huabei Hotel

Location D: Lotus Glade Hotel 52

Location E: Jinxi Hotel(Venue)

Click here to view large map.



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Registration

Symposium Registration Fees

ATS Registration	Advance,Before Oct. 24(US$)	Late,After Oct. 24/On Site(US$)
IEEE Member Fee	570.00	684.00
Non-Member Fee	684.00	821.00
Student Member Fee	314.00	376.00
Student Non-Member Fee	570.00	684.00
IEEE Life Member Fee	314.00	376.00

A full registration is required for each accepted paper by September 15.

- Only full registration includes the social event and banquet.
- **WRTLT** and **ATS** registrations are separate. Go to the WRTLT website for registration information.

Invitation letter for visa application:

Please contact: ats14@ict.ac.cn, if you need an invitation letter for visa application.

Tutorial Fees

ATS 2014 features two half-day tutorials on Nov. 16, 2014.

TUTORIAL I:

"Test, Diagnosis, and Root-Cause Identification of Failures for Boards and Systems"

Prof. Krishnendu Chakrabarty, Dept. of Electrical and Computer Engineering, Duke University

TUTORIAL II:

"Statistical Adaptive Test Methods Targeting 'Zero Defect' IC Quality and Reliability"

Prof. Adit D. Singh, Dept. of Electrical and Computer Engineering, Auburn University

Tutorial Registration		**Advance, Before** Oct.24(US$)	Late, After Oct. 24/On Site(US$)
Tutorial I & II	IEEE Member Fee	200.00	240.00
	Non-Member Fee	240.00	290.00
	Student Fee	110.00	130.00
Only Tutorial I	IEEE Member Fee	150.00	180.00
	Non-Member Fee	190.00	220.00
	Student Fee	80.00	100.00

Only Tutorial II	IEEE Member Fee	150.00	180.00
	Non-Member Fee	190.00	220.00
	Student Fee	80.00	100.00

Extra Page Fees for Regular Papers

- ATS'14 regular papers are allotted 6 pages free of charge. Each additional page beyond 6 pages will charge US$ 160. A maximum of 2 additional pages is allowed.
- Pay for the extra page charges in the online registration system when you make the symposium registration.

Extra Social Event Ticket

- US$90 per ticket

Registration Cancellation Policy

- All refunds/cancellation requests must be provided in writing and received by October 31, 2014.
- There will be an administration fee of US$ 150 deducted from each refund.
- Please submit all requests to Shufeng Liu by e-mail (ats14@ict.ac.cn).

Registration

- Click 

for online registration.
- Online registration requires major credit card account.
  Please Contact ats14@ict.ac.cn if you need any assistance.

国内代表注册，请点击进入

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Keynote & Invited Talks

Keynote Speaker

Prof. Shawn Blanton

Department of Electrical and Computer Engineering

Carnegie Mellon University

Title: Improving Design, Manufacturing, and Even Test through Test-Data Mining

Abstract: Since yield is not 100%, the main objective of test has and continues to be screening out bad ICs. Today, however, test is being used to provide valuable information about failing chips, answering questions about whether the design, the fabrication process or some combination of the two is responsible for failure. The information extracted is, ideally, used to improve design, fabrication and even test itself. In this talk, an overview of research in the Carnegie Mellon Advanced Chip Testing Laboratory in this area will be described with particular emphasis on one methodology that focuses on measuring the effectiveness of any fault model or test metric using normally-available test data. Experiment results from manufactured chips from both IDMs and chip-design houses will be used to illustrate the potential of this approach.

Biography: Shawn Blanton is a professor in the Department of Electrical and Computer Engineering at Carnegie Mellon University where he serves as director of the Center for Silicon System Implementation (CSSI), an organization consisting of 18 faculty members and over 80 students focused on the design and manufacture of silicon-based systems. He received the Bachelor's degree in engineering from CalvinCollege in 1987, a Master's degree in Electrical Engineering in 1989 from the University of Arizona, and a Ph.D. degree in Computer Science and Engineering from the University of Michigan, Ann Arborin 1995.

Professor Blanton's research interests are housed in the Advanced Chip Testing Laboratory (ACTL) and include the design, verification, test and diagnosis of integrated, heterogeneous systems. He has published many papers in these areas and has several issued and pending patents in the area of IC test and diagnosis. Prof. Blanton has received the National Science Foundation Career Award for the development of a microelectromechanical systems (MEMS) testing methodology and two IBM Faculty Partnership Awards. He is a Fellow of the IEEE, and is the recipient of the 2006 Emerald Award for outstanding leadership in recruiting and mentoring minorities for advanced degrees in science and technology.

Invited Talk

Mr. Greg Aldrich

Marketing Director at Mentor Graphics

Title: Transformation of DFT: From Load Board to Dashboard

Abstract: With the invention of scan in the late 70's, design-for-test and test generation technologies were originally relegated to a screening task for detecting manufacturing defects in processed wafers and packaged devices. Technology advances added sophisticated defect analysis capabilities, boosting the value of DFT as a critical part of yield ramp up.Today as digital electronics become more and more prevalent in safety critical functions within the automotive, aerospace, medical and similar industries, the role and value DFT plays in the design cycle and manufacturing process continues to increase and transform. In a quest to satisfy new safety standards like ISO26262 and DO-254, electronics systems manufacturers are looking for new technologies to ensure that electronic subsystems are defect free and fully functional – throughout the life of the system. Design-for-test technologies are already supporting these stringent requirements with capabilities such as built-in self-test (BIST) and power-on test. As technologies like fly-by-wire and the driverless car become reality, DFT will become an even more crucial player in support of real-time system level safety standards. The speaker will review the evolution of DFT technologies that have occurred in the past and discuss where future technologies can further expand the scope and value of DFT.

Biography: Greg Aldrich is the Director of Marketing for the Silicon Test Solutions product group at Mentor Graphics. Previously, Aldrich held a variety of technical and product marketing positions at Mentor Graphics. Prior to joining Mentor, Aldrich served in various engineering and marketing roles at Interconnectix (Beaverton, Oregon), Sunrise Test Systems (San Jose, California), and Amdahl Corporation (Sunnyvale, California). He holds a bachelor's degree in Electrical Engineering from the University of Illinois at Urbana-Champaign.

Qing-Qing Sun

Fudan University

Title: The Characterization Challenges in Modeling Semi-Floating Gate Transistors

Abstract: Semi-Floating gate transistors (SFGT) is a new type of semiconductor device with potential applications in Dynamic Read Access Memories (DRAM) and CMOS Image Sensors (CIS). The operation speed of SFGT is almost in the same level of traditional SRAM which has the operation speed below 1 ns. Although SFGT shows attractive performance due to its fast speed and low power consumption, the ERASE/READ/WRITE/READ operation of SFGT is rather complicate which introduce

many challenges in device characterizations. In this report, we will firstly talk about the operation scheme of SFGT during the READ/ERASE/WRTIE and shows the performance of the device we get with our test methodology. Secondly, we will discuss the challenges and accuracy of the test methods when device is operated at ultra-high speed.

Biography: Qing-Qing Sun received his Ph.D. degrees in microelectronics and solid state electronics from Fudan University, Shanghai, in 2009. He received B.S. (2004), Fudan University, in Physics. In 2009 he joined the department of microelectronics, Fudan University, as a Lecturer. He was promoted to be Associate Professor and Full Professor in 2011 and 2013, respectively. He has authored or co-authored more than 90 papers in journals and conferences and awarded more than 20 patents. His research interests include novel semiconductor devices, atomic layer deposition, resistive switching memories and advanced interconnect technology.

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Tutorial

- **TUTORIAL I:**
  "**Test, Diagnosis, and Root-Cause Identification of Failures for Boards and Systems** "
  Prof. Krishnendu Chakrabarty, Dept. of Electrical and Computer Engineering, Duke University
- **TUTORIAL II:**
  "**Statistical Adaptive Test Methods Targeting 'Zero Defect' IC Quality and Reliability**"
  Prof. Adit D. Singh, Dept. of Electrical and Computer Engineering, Auburn University

Tutorial I		
Title	**Test, Diagnosis, and Root-Cause Identification of Failures for Boards and Systems**	
Presenter	*Prof. Krishnendu Chakrabarty* *Dept. of Electrical and Computer Engineering,* *Duke University*	

Biography

Krishnendu Chakrabarty is the William H. Younger Distinguished Professor of Engineering in the Department of Professor of Electrical and Computer Engineering and Professor of Computer Science at Duke University. In addition, he serves as the Executive Director of Graduate Studies in Electrical and Computer Engineering. He is also a Chair Professor at Tsinghua University, Beijing, China. Prof. Chakrabarty is a recipient of the National Science Foundation Early Faculty (CAREER) award, the Office of Naval Research Young Investigator award, the Humboldt Research Award from the Alexander von Humboldt Foundation, Germany, and 10 best paper awards at major IEEE conferences. He is also a recipient of the Distinguished Alumnus Award from the Indian Institute of Technology, Kharagpur (2014).

Prof. Chakrabarty's current research projects include: testing and design-for-testability of integrated circuits; digital microfluidics, biochips, and cyberphysical systems; optimization of digital print and enterprise systems. Prof. Chakrabarty is a Fellow of ACM, a Fellow of IEEE, and a Golden Core Member of the IEEE Computer Society. He holds four US patents and he has several pending patents. He was a 2009 Invitational Fellow of the Japan Society for the Promotion of Science (JSPS). He served as a Distinguished Visitor of the IEEE Computer Society during 2005-2007 and 2010-2012, and as a Distinguished Lecturer of the IEEE Circuits and Systems Society during 2006-2007 and 2012-2013. Currently he serves as an ACM Distinguished Speaker.

Prof. Chakrabarty served as the Editor-in-Chief of IEEE Design & Test of Computers during 2010-2012. Currently he serves as the Editor-in-Chief of ACM Journal on Emerging Technologies in Computing Systems. He is also an Associate Editor of IEEE Transactions on Computers, IEEE Transactions on Biomedical Circuits and Systems, and ACM Transactions on Design Automation of Electronic Systems.

Abstract

The gap between working silicon and a working board/system is becoming more significant and problematic as technology scales and complexity grows. The result of this increasing gap is failures at the board and system level that cannot be duplicated at the component level. These failures are most often referred to as “NTFs” (No Trouble Founds). The result of these NTFs can range from higher manufacturing costs and inventories to failure to get the product out of the door. The problem will only get worse as technology scales and will be compounded as new packaging techniques (SiP, SoC, 3D) extend and expand Moore’s law. This is a problem that must be solved, yet, little effort has been applied up to this point. This tutorial will provide a detailed background on the nature of this problem and will provide DFT, test, and root-cause identification solutions at the board/system level.

Tutorial II

Title	**Statistical Adaptive Test Methods Targeting 'Zero Defect' IC Quality and Reliability**	
Presenter	*Prof. Adit D. Singh* *Dept. of Electrical and Computer Engineering, Auburn University*	

Biography

Adit D. Singh is James B. Davis Professor of Electrical and Computer Engineering at Auburn University, where he directs the VLSI Design and Test Laboratory. His technical interests span all aspects of VLSI test and reliability. He has published nearly two hundred research papers, served as a consultant for several major semiconductor companies, and holds international patents that have been licensed to industry. He has held leadership roles at international test conferences, including serving as General Chair of the 2000 IEEE VLSI Test Symposium, the 2003 IEEE Defect Based Test Workshop, and the 2004 IEEE Memory Test Workshop. He also serves on the editorial boards of IEEE Design and Test Magazine, and JETTA. Dr. Singh is a Fellow of IEEE, a Golden Core member of the IEEE Computer Society and is past chair of the IEEE Test Technology Technical Council. He can be reached at email: adsingh@auburn.edu.

Abstract

Integrated circuits fabricated in aggressively scaled nanometer scale technologies are susceptible to a wide range of random manufacturing defects, some of which can be extremely difficult to reliably detect in post manufacturing testing. Meanwhile commercial applications continue to demand ever higher IC quality, most notably a “zero defect ” target from automotive manufacturers. To cost effectively meet these new quality and reliability challenges, innovative new statistical screening techniques and adaptive test methodologies are being developed. These attempt to improve test effectiveness and optimize test costs by identifying “suspect” parts for more extensive testing, using tests specially targeted at the suspected failure mode. Adaptive test methods fall into two broad categories: those that exploit the statistics of defect distribution on wafers, and those that exploit the correlation in the variation of process and performance parameters on wafers. This tutorial presents test methodologies that span both these categories, and illustrates their effectiveness with results from a number of recently published experimental studies on production digital and analog circuits. Commercial tools offered by a number of new companies that have emerged in the "Adaptive Test" space will also be discussed. Broadly, these aim provide to support for the sharing and leveraging of results from the different tests in the test flow for effective test

adaptation and optimization.

ATS'14

November 16-19, 2014. Hangzhou, China

The 23rd Asian Test Symposium

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Nov. 16

8:30am – 12:00pm

Tutorial I: Test, Diagnosis, and Root-Cause Identification of Failures for Boards and Systems
Prof. Krishnendu Chakrabarty, Duke University

2:00pm-6:00pm

Tutorial II: Statistical Adaptive Test Methods Targeting 'Zero Defect' IC Quality and Reliability
Prof. Adit D. Singh, Auburn University

Nov. 17

8:30am – 9:00am

Opening Session

9:00am – 10:00am

Keynote: Improving Design, Manufacturing, and Even Test through Test-Data Mining
Prof. Shawn Blanton, Carnegie Mellon University

10:00am – 10:30am Coffee break

10:30am – 11:15am

Invited talk I: Transformation of DFT: From Load Board to Dashboard
Mr. Greg Aldrich, Marketing Director at Mentor Graphics

11:15am – 12:00pm

Invited talk II: The Characterization Challenges in Modeling Semi-Floating Gate Transistors
Prof. David Wei Zhang, Fudan University

12:00pm – 1:30pm Lunch

1:30pm – 2:45pm Session 1A/1B/1C

Session 1A: 3D Testing

Session Chair: Li Jiang, Shanghai Jiao Tong University

- BIST-Assisted Tuning Scheme for Minimizing IO-Channel Power of TSV-Based 3D DRAMs

Yun-Chao Yu[1], Chi-Chun Yang[1], Jin-Fu Li[1], Chih-Yen Lo[2], Chao-Hsun Chen[2], Jenn-Shiang Lai[2], Ding-Ming Kwai[2], Yung-Fa Chou[2], and Cheng-Wen Wu[3]

[1]Department of Electrical Engineering National Central University

[2]Information and Communication Research Lab. Industrial Technology Research Institute

[3]Department of Electrical Engineering, National Tsing Hua University

- **Dual-Speed TAM Optimization of 3D SoCs for Mid-Bond and Post-Bond Testing**

Kele Shen[1], Dong Xiang[2] and Zhou Jiang[2]

[1]Department of Computer Science, Tsinghua University

[2]School of Software, Tsinghua University

- **Optimized Pre-bond Test Methodology for Silicon Interposer Testing**

Katherine Shu-Min Li[1], Sying-Jyan Wang[2], Jia-Lin Wu[1], Cheng-You Ho[1], Yingchieh Ho[3], Ruei-Ting Gu[1,4], Bo-Chuan Cheng[4]

[1]Department of Computer Science, National Sun Yat-sen University, Kaohsiung, Taiwan

[2]Department of Computer Science, National Chung Hsing University, Taichung, Taiwan

[3]Department of Electrical Engineering, National Dong Hwa University, Hualien, Taiwan

[4]Advanced Semiconductor Engineering (ASE) Group, Kaohsiung, Taiwan

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Session 1B: Reliability

Session Chair: Zhiyuan Wang, Huawei Corp.

- **Design of a Radiation Hardened Latch for Low-power Circuits**

Huaguo Liang[1], Zhi Wang[1], Zhengfeng Huang[1], and Aibin Yan[2]

[1]School of Electronic Science and Applied Physics, Hefei University of Technology, Hefei 230009, P.R. China

[2]School of Computer and Information, Hefei University of Technology, Hefei 230009, P.R. China

- **Optimal Redundancy Designs for CNFET-Based Circuits**

Da Cheng, Fangzhou Wang, Feng Gao, and Sandeep K. Gupta

Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles, CA, USA

- **A Heuristically Mechanical Model for Accurate and Fast Soft Error Analysis**

Jiajia Jiao, Yuzhuo Fu

School of Micro Electronics, Shanghai Jiao Tong University, Shanghai, China

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Special Session 1C: Resilient Circuit Design and Test

Moderator: Mehdi Tahoori, Karlsruhe Institute of Technology, Germany

- Error Resilient Real-Time State Variable Systems for Signal Processing and Control

Suvadeep Banerjee[1], A´ lvaro Go´mez-Pau[2], Abhijit Chatterjee[1] and Jacob A. Abraham[3]

[1]School of Electrical and Computer Engineering, Georgia Institute of Technology

[2]Universitat Polit`ecnica de Catalunya, Barcelona, Spain

[3]Electrical and Computer Engineering, University of Texas at Austin

- **Variability and Soft-Error Resilience in Dependable VLSI Platform**

Yukio Mitsuyama[1] , and Hidetoshi Onodera[2],

[1]Kochi University of Technology, [2] Kyoto University

- **Adaptive Mitigation of Parameter Variations**

1 2 1 2 1

Farshad Firouzi , Fangming Ye , Saman Kiamehr , Krishnendu Chakrabarty , and Mehdi B. Tahooriy
[1]Karlsruhe Institute of Technology, Germany
[2]Department of Electrical and Computer Engineering, Duke University, Durham, NC, USA

2:45pm – 3:15pm Coffee break

3:15pm – 4:30pm Session 2A/2B/2C

Session 2A: Testing of Emerging Technologies

Session Chair: Sandeep Gupta, Univ. of Southern California

- **Reliability-Driven Pipelined Scan-Like Testing of Digital Microfluidic Biochips**

Zipeng Li[1], Trung Anh Dinh[2], Tsung-Yi Ho[3], Krishnendu Chakrabarty[1]

[1]Department of Electrical and Computer Engineering, Duke University, Durham, NC, USA

[2]Graduate School of Information Science and Engineering, Ritsumeikan University, Shiga, Japan

[3]Computer Science Department, National Chiao Tung University, Hsinchu, Taiwan

- **A Cost-Effective Stimulus Generator for Battery Channel Characterization in Electric Vehicles**

Shao-Feng Hung, Long-Yi Lin, and Hao-Chiao Hong

Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan

- **Generator for Test Set Construction of SMGF in Reversible Circuit by Boolean Difference Method**

Bappaditya Mondal[1], Dipak Kumar Kole[1], Debesh Kumar Das[2] and Hafizur Rahaman[1]

[1]Department of Information Technology, Indian Institute of Engineering Science and Technology, Shibpur, India

[2]Department of Computer Science and Engineering, Jadavpur University, Kolkata, India

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Session 2B: SoC Testing

Session Chair: Yu Huang, Mentor Graphics

- **High-Speed Serial Embedded Deterministic Test for System-on-Chip Designs**

Maciej Trawka Grzegorz Mrugalski[1], Nilanjan Mukherjee[1], Artur Pogiel[2], Janusz Rajski[2]
Jakub Janicki[3], Jerzy Tyszer[3]
[1]Gdańsk University of Technology, 80-233 Gdańsk, Poland
[2]Mentor Graphics Corporation, Wilsonville, OR 97070, USA
[3]Poznań University of Technology, 60-965 Poznań, Poland

- **A Scalable and Parallel Test Access Strategy for NoC-Based Multicore System**

Taewoo Han, Inhyuk Choi, Hyunggoy Oh, Sungho Kang
Department of Electrical and Electronic Engineering, Computer systems & reliable SoC Lab., Yonsei University, Seoul, Korea

- **On Covering Structural Defects in NoCs by Functional Tests**

Atefe Dalirsani, Nadereh Hatami, Michael E. Imhof, Marcus Eggenberger, Gert Schley,
Martin Radetzki, Hans-Joachim Wunderlich
Institute of Computer Architecture and Computer Engineering, University of Stuttgart, Germany

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Special Session 2C: Design, Verification and Application of IEEE 1687

Moderator: Erik Larsson, Lund University, Sweden

- **Design, Verification and Application of IEEE 1687**
  Farrokh Ghani Zadegan[1], Erik Larsson[1], Artur Jutman[2], Sergei Devadze[2] *3*
  [1]Lund University, Lund, Sweden
  [2]Testonica Lab, Tallinn, Estonia
  [3]Hochschule Hamm-Lippstadt, Hamm, Germany

4:30pm – 5:00pm Coffee break

5:00pm – 6:40pm Session 3A/3B/3C

Session 3A: Post-Silicon Validation

Session Chair: Michael Hsiao, Virginia Tech.

- **Silicon Evaluation of Cell-Aware ATPG Tests and Small Delay Tests**
  Fan Yang[1], Sreejit Chakravarty[1], Arun Gunda[1], Nicole Wu[2] and Jianyu Ning[2]
  [1]Avago Technologies, San Jose, CA, USA
  [2]Avago Technologies, Shanghai, China

- **On Supporting Sequential Constraints for On-Chip Generation of Post-Silicon Validation Stimuli**
  Xiaobing Shi and Nicola Nicolici
  Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada

- **Predicting IC Defect Level using Diagnosis**
  Cheng Xue and R.D. (Shawn) Blanton
  ECE Department, Carnegie Mellon University, Pittsburgh, PA, USA

Session 3B: Testability and Test Generation

Session Chair: Hans-Joachim Wunderlich, University of Stuttgart

- **Testability-Driven Fault Sampling for Deterministic Test Coverage Estimation of Large Designs**
  Kun-Han Tsai
  Mentor Graphics Corporation, Wilsonville, OR 97070, USA

- **Methodology for Early RTL Testability and Coverage Analysis and Its Application to Industrial Designs**
  Chandan Kumar[1], Fadi Maamari[1], Kiran Vittal[1], Wilson Pradeep[2], Rajesh Tiwari[2], Srivaths Ravi[2]
  [1]Atrenta Inc., San Jose, U.S.A
  [2]Texas Instruments Inc., Bengaluru, India

- **Circuit Parameter Independent Test Pattern Generation for Interconnect Open Defects**
  Dominik Erb[1], Karsten Scheibler[1], Matthias Sauer[1], Sudhakar M. Reddy[2], Bernd Becker[1]
  [1]Chair of Computer Architecture, University of Freiburg, Germany
  [2]Dept. of ECE, University of Iowa, USA

Session 3C: TTTC's Doctoral Thesis Award: Asian Semi-Final

Session Chair: Jiun-Lang Huang, National Taiwan University

- **Researching on the critical techniques of metamorphic testing to provide more effective test**

oracle
Zhan-Wei Hui,
PLA Univ. of Science and Technology

- **Yield and reliability enhancement for 3D ICs**
Li Jiang,
The Chinese University of Hong Kong

- **An analytical model driven framework for accurate and efficient soft error analysis in processors**
Jiajia Jiao,
Shanghai Jiao Tong University

- **Diagnosis techniques for identifying faults in digital VLSI system**
Subhadip Kundu,
IIT Kharagpur

- **Multiple-fault-oriented fault diagnosis for digital integrated circuits**
Jing Ye,
Institute of Computing Technology, Chinese Academy of Sciences

Nov. 18

9:00am – 10:15am Session 4A/4B/4C

Session 4A: Yield Optimization of Memory

Session Chair: Jin-Fu Li, National Central University

- **Built-In Scrambling Analysis for Yield Enhancement of Embedded Memories**

Shyue-Kung Lu[1], Hao-Cheng Jheng[1], Hao-Wei Lin[1], Masaki Hashizume[2], and Seiji Kajihara[3]

[1]Dept. Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan

[2] Institute of Technology and Science, The University of Tokushima, Tokushima, Japan

[3]Dept. Creative Informatics, Kyushu Institute of Technology, Kyushu, Japan

- **Intra-Channel Reconfigurable Interface for TSV and Micro Bump Fault Tolerance in 3-D RAMs**

Kuan-Te Wu[1], Jin-Fu Li[1], Yun-Chao Yu[1], Chih-Sheng Hou[1], and Chi-Chun Yang[1], Ding-Ming Kwai[2], Yung-Fa Chou[2] and Chih-Yen Lo[2]

[1]Department of Electrical Engineering, National Central University, Taoyuan, Taiwan 320

[2]Information and Communication Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan 310

- **SRAM array yield Estimation under spatially-correlated process variation**

Jizhe Zhang and Sandeep Gupta

Department of Electrical Engineering, University of Southern California

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Session 4B: On-Line Parameter Testing

Session Chair: Xiaoxiao Wang, Beihang University

- **Temperature and Voltage Estimation Using Ring-Oscillator-Based Monitor for Field Test**

Yousuke Miyake[1], Yasuo Sato[1], Seiji Kajihara[1]and YukiyaMiura[2]

[1]Kyushu Institute of Technology, Iizuka, Japan

[2]Tokyo Metropolitan University, Tokyo, Japan

- **On-Line Transition-Time Monitoring for Die-to-Die Interconnects in 3D ICs**

Shi-Yu Huang[1], Hua-Xuan Li[1], Zeng-Fu Zeng[1], Kun-Han Tsai[2], and Wu-Tung Cheng[2]

1

Electrical Engineering Department, National Tsing Hua University, Taiwan

[2]Silicon Test Solutions, Mentor Graphics

- **A Novel Circuit for Transition-Edge Detection: Using a Stochastic Comparator Group to Test Transition-Edge**

Takahiro J. Yamaguchi[1,3], James S. Tandon[2,3], Satoshi Komatsu[3,4], Kunihiro Asada[3]

[1]Advantest Laboratories, Ltd., Sendai, Miyagi, Japan

[2]Microsemi, San Jose, CA, USA

[3]D2T, VDEC, The University of Tokyo, Tokyo, Japan

[4]School of Engineering, Tokyo Denki University, Tokyo, Japan

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Session 4C: Embedded Tutorial-Hierarchical Scan Compression 1

Yu Huang, Mentor Graphics

ZhenXin Sun, Cadence

Ang Li, Synopsys

10:15am – 10:45am Coffee break

10:45am – 12:00pm Session 5A/5B/5C

Session 5A: Power/Temperature-Aware Testing

Session Chair: Seiji Kajihara, Kyushu Institute of Technology

- **Low Power Test Compression with Programmable Broadcast-Based Control**

Sylwester Milewski[1], Grzegorz Mrugalski[2], Janusz Rajski[2], Jerzy Tyszer[1]

[1]Poznań University of Technology, 60-965 Poznań, Poland

[2]Mentor Graphics Corporation, Wilsonville, OR 97070, USA

- **Exploit Dynamic Voltage and Frequency Scaling for SoC Test Scheduling under Thermal Constraints**

Li Ling, Jianhui Jiang

School of Software Engineering, Tongji University, Shanghai, China

- **High Quality Testing of Grid Style Power Gating**

Vasileios Tenentes[1], Saqib Khursheed[2], Bashir M. Al-Hashimi[1], Shida Zhong[1], Sheng Yang[1]

[1]ECS, University of Southampton, UK.

[2]Electrical Engineering & Electronics, University of Liverpool, UK.

Session 5B: Trojan/Fault Detection with High Resolution

Session Chair: Katherine Shu-Min Li, National Sun Yat-Sen University

- **A Resizing Method to Minimize Effects of Hardware Trojans**

Byeongju Cha and Sandeep K. Gupta

Ming Hsieh Department of Electrical Engineering, University of Southern California Los Angeles, USA

- **High Resolution Pulse Propagation Driven Trojan Detection In Digital Logic: Optimization Algorithms and Infrastructure**

Sabyasachi Deyati[1] ,Barry John Muldrey[1], Adit Singh[2], Abhijit Chatterjee[1]

[1]Electrical & Computer Engineering, Georgia Institute of Technology, Atlanta GA 30332, USA

[2]Department of Electrical Engineering, Auburn University, AL 36849, USA

- **Physically-Aware Diagnostic Resolution**
  John A. Porche, R. D. (Shawn) Blanton
  Dept. of ECE Carnegie Mellon University Pittsburgh, PA 15213

Session 5C: Embedded Tutorial- Hierarchical Scan Compression 2

Yu Huang, Mentor Graphics

ZhenXin Sun, Cadence

Ang Li, Synopsys

12:00pm – 1:30pm Lunch

1:30pm – 3:10pm Session 6A/6B/6C

Session 6A: Analog/Memory Testing

Session Chair: Jiun-Lang Huang, National Taiwan University

- **On-chip implementation of an Integrator-Based servo-loop for ADC static linearity test**
  Guillaume Renaud[1], Manuel J. Barragan[1], and Salvador Mir[1], Marc Sabut[2]
  [1]Universite Grenoble Alpes, TIMA, F-38000 Grenoble, France ´ CNRS, TIMA, F-38000 Grenoble, France
  [2]STMicroelectronics Grenoble 12, Rue Jules Horowitz, F-38000 Grenoble, France

- **An ATE Based 32 Gbaud PAM-4 At-Speed Characterization and Testing Solution**
  Jose Moreira[1], Hubert Werkmann[1], Masahiro Ishida[1], Bernhard Roth[1], Volker Filsinger[2], Sui-Xia Yang[1]
  [1]Advantest
  [2]SHF Communication Technologies

- **Testing of Non-Volatile Logic-Based System Chips**
  Yong-Xiao Chen and Jin-Fu Li
  Advanced Reliable Systems (ARES) Lab, Department of Electrical Engineering, National Central University, Jhongli, Taiwan 320

- **Dual-Purpose Mixed-Level Test Generation Using Swarm Intelligence**
  Kelson Gent and Michael S. Hsiao
  Bradley Department of Electrical and Computer Engineering Virginia Tech, Blacksburg, VA 24061, USA

Panel Session 6B: Big Data for Test

Moderators: K.-T. Tim Cheng, University of California, Santa Barbara

Harry H. Chen, MediaTek Inc.

- **Learning from Production Test Data: Correlation Exploration and Feature Engineering**
  Fan Lin, Chun-Kai Hsu, and Kwang-Ting Cheng
  Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106

- **Leveraging Big Data Analytics to Drive Failure Analysis in Manufacturing Operations**
  David Park,
  Optimal+

- **Data Driven Design Centric Yield Learning**
  John Kim,
  Synopsys

- **Perspectives on Test Data Mining from Industrial Experience**
  Harry H. Chen,
  Design Technology Department, MediaTek Inc. Hsinchu, Taiwan

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Special Session 6C: In-Field Techniques for Performance Adaption, Test, and Power-Noise Diagnosis

Moderator: Xiaoqing Wen, Kyushu Institute of Technology, Japan

- **Opportunities and Verification Challenges of Run-time Performance Adaptation**
  Masanori Hashimoto
  Dept. Information Systems Engineering, Osaka University

- **An On-Chip Digital Environment Monitor for Field Test**
  Seiji Kajihara, Yousuke Miyake, Yasuo Sato, Yukiya Miura
  Kyushu Institute of Technology

- **On-Chip Monitoring for In-Place Diagnosis of Undesired Power Domain Problems in IC Chips**
  Makoto Nagata, Daisuke Fujimoto, Noriyuki Miura
  Graduate School of System Informatics, Kobe University, Japan

3:30pm – 10:00pm Social Event & Banquet

Nov. 19

9:00am – 10:15am Session 7A/7B/7C

Session 7A: Timing Variation Detection

Session Chair: Shi-Yu Huang, National Tsinghua University

- **An On-Line Timing Error Detection Method for Silicon Debug**

Yun Cheng[1,2], Huawei Li[1], Xiaowei Li[1]

[1]State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

[2]University of Chinese Academy of Sciences, Beijing, China

- **An All Digital Distributed Sensor Network Based Framework for Continuous Noise Monitoring and Timing Failure Analysis in SoCs**

Mehdi Sadi [1], Zoe Conroy [2], Bill Eklow [2], Matthias Kamm [2], Nematollah Bidokhti [2] and Mark (Mohammad) Tehranipoor [1]

[1]Dept. of Electrical & Computer Engineering, University of Connecticut, Storrs, USA

[2]Cisco Systems, San Jose, CA, USA

- **On-Chip Delay Sensor for Environments with large Temperature Fluctuations**

Jibing Qiu, Guihai Yan, Xiaowei Li

State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

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Session 7B: Delay Testing

Session Chair: Bernd Becker, University of Freiburg

- **Timing Evaluation Tests for Scan Enable Signals with Application to TDF Testing**
  Jie Zou, Chao Han and Adit D. Singh
  Department of Electrical and Computer Engineering, Auburn University, Auburn AL, 36849

- **FPGA-Based Subset Sum Delay Lines**

  Chung-Yun Wang[1], Yu-Yi Chen[1], Jiun-Lang Huang[1], Xuan-Lun Huang[2]

  [1]Graduate Institute of Electronics Engineering, Department of Electrical Engineering, National Taiwan University

  [2]Industrial Technology Research Institute, Hsinchu, Taiwan

- **Parallel Path Delay Fault Simulation for Multi/Many-Core Processors with SIMD Units**

  Yussuf Ali[1] Yuta Yamato[1] Tomokazu Yoneda[1] Kazumi Hatayama[2] Michiko Inoue[1]

  [1] Nara Institute of Science and Technology, Nara, Japan

  [2]Gunma University, Gunma, Japan

Special Session 7C: High Quality System Level Test and Diagnosis

Moderator: Hans-Joachim Wunderlich, University of Stuttgart

- **High Quality System Level Test and Diagnosis**

  Artur Jutman[1], Matteo Sonza Reorda[2], Hans-Joachim Wunderlich[3]

  [1]Testonica Lab, Tallinn, Estonia, [2]Politecnico di Torino, Italy, [3]University of Stuttgart, Germany

10:15am – 10:45am Coffee break

10:45am – 12:00pm Session 8A/8B/8C

Session 8A: Diagnosis

Session Chair: Sybille Hellebrand, University of Paderborn

- **An Efficient Diagnosis Pattern Generation Procedure to Distinguish Stuck-at Faults and Bridging Faults**

  Cheng-Hung Wu and Kuen-Jong Lee

  Dept. of EE, National Cheng Kung University, Taiwan

- **On the Generation of Diagnostic Test Set for Intra-cell Defects**

  Z. Sun[1], A. Bosio[1], L. Dilillo[1], P. Girard[1], A. Virazel[1], E. Auvray[2]

  [1]LIRMM UM2-CNRS, Montpellier, France

  [2]ST Microelectronics, Grenoble, France

- **Diagnosing Cell Internal Defects Using Analog Simulation-based Fault Models**

  Huaxing Tang[1], Brady Benware[1], Michael Reese[2], Joseph Caroselli[2], Thomas Herrmann[3], Friedrich Hapke[4], Robert Tao[2], Wu-Tung Cheng[1], Manish Sharma[1]

  [1]Mentor Graphics, Wilsonville, Oregon, USA

  [2]AMD, Inc. Austin, Texas, USA

  [3]GLOBALFOUNDRIES, Dresden, Germany

  [4]Mentor Graphics, Hamburg, Germany

Session 8B: Test Compression

Session Chair: Huaguo Liang, Hefei University of Technology

- **Improving Output Compaction Efficiency with High Observability Scan Chains**

  Sying-Jyan Wang[1], Che-Wei Kao[1], Katherine Shu-Min Li[2]

  [1]Department of Computer Science and Engineering, National Chung Hsing University, Taichung, Taiwan

  [2]Department of Computer Science and Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan

- **Two-Step Dynamic Encoding for Linear Decompressors**

  Emil Gizdarski

  Synopsys Inc., 700 East Middlefield Road, Mountain View, CA 94043

- **A Case Study on Implementing Compressed DFT Architecture**
  A. Chandra, S. Chebiyam, and R. Kapur
  Synopsys, Inc., 700 E. Middlefield Rd., Mountain View, CA, 94043, USA

Special Session 8C: Hardware Security

Moderator: Yier Jin, University of Central Florida

- **Leveraging Emerging Technology for Hardware Security - Case Study on Silicon Nanowire FETs and Graphene SymFETs**
  Yu Bi[1], Pierre-Emmanuel Gaillardon[2], X. Sharon Huz[3], Michael Niemierz[3], Jiann-Shiun Yuan[1], and Yier Jin[1]
  [1]Department of Electrical Engineering and Computer Science, University of Central Florida
  [2]Ecole Polytechnique F ´ ed´ erale de Lausanne (EPFL) - Switzerland ´
  [3]Department of Computer Science and Engineering, University of Notre Dame

- **Advanced Analysis of Cell Stability for Reliable SRAM PUFs**
  Alison Hosey, Md. Tauhidur Rahman, Kan Xiao, Domenic Forte, and Mohammad Tehranipoor
  ECE Department, University of Connecticut

- **On the Use of Scan Chain to Improve Physical Attacks**
  Junfeng Fan[1], Hua Xie[2], Yiwei Zhang[2]
  [1]Nationz technologies and Open Security Research, Shenzhen, China
  [2]Nationz technologies, Shenzhen, China

ATS'14
November 16-19, 2014. Hangzhou, China
The 23rd Asian Test Symposium

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- WRTLT'14
- ATS History

INSTRUCTIONS FOR SPEAKERS OF REGULAR SESSIONS/SPECIAL SESSIONS/EMBEDDED TUTORIAL

This page provides instructions for speakers of regular papers/special sessions/embedded tutorial. Panel speakers should contact their session organizers and/or moderators for further information.

Presentation Time:

Regular Paper/Special Sessions/Embedded Tutorial:

- Your paper is allotted 25 minutes as follows:

  (i) 2 minutes for introduction, set up etc.

  (ii) 20 minutes for presentation, and

  (iii) 3 minutes for Q&A.

Presentation Preparation Guide:

- *October 31* is the deadline to submit your presentation file and related information to the ATS 2014 system. *http://www.carch.ac.cn/ats2014/submitSlides/*
- Only *PowerPoint* files are accepted, which will be played on *Microsoft Windows XP*.
  - Focus on pertinent information
  - DO NOT attempt to fit entire paper onto slides
  - List only the key innovations and novel approaches on slides
  - Get straight to the point, audience comprises of technical experts
  - Details of proofs, previous works, and theories are redundant
  - *High contrast: Light lettering/lines on a dark background*
    - Foreground: White, yellow, light cyan
    - Background: Black, dark blue, brown, dark green
    - Caution: Red, orange or blue lettering and lines become unreadable when projected
  - Short phrases, not long sentences: 36 point titles and 28 point text recomended
  - Use large font sizes. 24 point and higher for regular text and 20 point for descriptive text.
  - Use graphs instead of tables
  - Use the width to height aspect ratio of most graphics displays is 4:3.
  - Your company name and/or logo are only allowed to appear on the title page. Also minimize the use of product trademarks.

- Do not use any sound effects.
- Spell check your slides!

At the Symposium:

- Meet with your Session Chair prior to your session. You can find out the name of your Session Chair in the ATS 2014 program booklet.
- Go through the exercise of familiarizing yourself with the audio-visual equipment prior to your session.
- If, for some reason, you are unable to contact your Session Chair, please contact the registration desk as soon as possible.

At your Session:

- Please be present in your session at least 15 minutes before the session starts.
- Test out your presentation on the symposium PC to make sure it works as expected.
- As a courtesy to other presenters and to the attendees, follow the time guidelines very closely. The Session Chair will give you a first reminder after 10 minutes have elapsed and a second reminder when only 2 minutes are left. Please use these reminders to pace your presentation appropriately, and ensure that you finish in the allotted 15/20 minutes.
- If there is any question that you do not understand, please ask the questioner or Session Chair to repeat or clarify. Lengthy discussions can be taken offline.

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INSTRUCTIONS TO SESSION CHAIRS

Thank you for your important contribution to ATS 2014. As "conductors" of the program, Session Chairs play an important role in ensuring that the sessions proceed in a smooth, timely, and interactive manner.

Time Limits:

Regular Session/Special Session/Embedded Tutorial: 25 minutes to be divided as follows:

(i) 2 minutes for introduction, set up etc.,

(ii) 20 minutes for presentation, and

(iii) 3 minutes for Q&A.

- Please ensure that the time limits are adhered to very strictly.
- Please give the authors two warnings during their presentation: (i) at the end of 10 minutes, and (ii) 2 minutes before the end of the presentation.

General Duties:

- The Session Chair will introduce the speakers, keep the time, and moderate the Q&A process.
- The Session Chair will assist the speakers with the audio-visual equipment, room lighting during the presentation, and get help from the A/V technicians in case it is needed.

Pre-Session Tasks:

- Depending on the timing of your session, you will meet with the presenters 15 minutes before the session starts.
- Report any missing speakers to the session room assistant as soon as possible.
- Please discuss with the authors the time limits for the papers. Inform them as to how you will communicate with them the progress of time. Stress the fact that time limits will be strictly adhered to.

For Each Speaker:

- Introduce the speaker.
- Keep track of time and give the speaker appropriate signals to alert the speaker.

Moderate the discussion by

- Reminding the audience to identify themselves and state their affiliations when asking a question.
- Clarifying questions if needed.
- Avoiding long discussions and suggesting that they be taken off-line
- Preventing any one individual from dominating the discussion
- Asking, if needed, a few questions of your own.

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ATS'14 Social event

Time: 3:30pm-10pm, Nov. 18

3:30pm A trip around the West Lake

Route of the trip: JinXi (金溪) – Quyuan Garden (曲院风荷) – Spring Dwan at Su Causeway (苏堤春晓) – Lingering Snow on the Broken Bridge (断桥残雪) – Louwailou (楼外楼)

6:00pm Banquet at the Hangzhou Louwailou restaurant

7:30pm A famous program played right on the West Lake: Impression of West Lake

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Introductions

- Introduction of Hangzhou, China

  http://www.hicenter.cn/

- Introduction of West Lake

  http://www.answers.com/topic/west-lake

- Introduction of the program: Impression of West Lake

Strong history and culture to the West Lake and the beautiful natural scenery as a source of creativity, in-depth digging Hangzhou, an ancient folk tales, myths, cultural and historical representation of the elements of the West Lake to reproduce the same time, re-use of high-tech way, "West Lake Rain", from a side of West Lake and West Lake in the rain to reflect the natural charm of the rain. The entire landscape virtual performances, through dynamic interpretation, realistic reproduction of the Hangzhou City connotation and condensed into a natural landscape to a high standard of art in the world, introduced to the world.

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Call for Papers (pdf)

The Asian Test Symposium (ATS) provides an open forum for researchers and industrial practitioners from all countries of the world, especially from Asia, to exchange innovative ideas on system, board, and device testing with design, manufacturing and field consideration in mind.

Scope

Original papers on, but not limited to, the following areas are invited.

- Automatic Test Pattern Generation
- Fault Modeling and Simulation
- Design Verification and Validation
- Diagnosis and Debug
- Board and System Test
- Analog/Mixed-Signal Test
- High-Speed I/O Test
- RF Test
- Delay and Performance Test
- Memory Test/FPGA Test
- System-in-Package/3D Test
- Software Testing
- Boundary Scan Test
- Built-In Self-Test
- Design-for-Testability
- Test Compression
- On-Line Test
- Temperature/Power-Aware Testing
- Defect-Based Testing
- Fault Tolerance
- Dependable System
- Yield Analysis and Enhancement
- Test Quality
- Economics of Test
- Hardware Security

Submissions

Regular Sessions: The ATS'14 Program Committee invites original, unpublished paper submissions on the above topics. Paper submissions should be complete manuscripts, not exceeding six pages (including figures, tables, and bibliography) in a standard IEEE two-column format. The submission will be considered evidence that upon acceptance the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication.

ATS'14 will present a Best Paper Award to a selected paper of exceptional quality. The evaluation will be conducted by an award committee constituted by experts covering all aspects of test technology, based on the criteria of innovation, potential impact, and presentation quality.

Key Dates

- Submission deadline: ~~May 16, 2014~~ May 23(extended)
- Notification of acceptance: Aug. 10, 2014

Camera ready manuscript: Sept. 5, 2014

Diamond Supporter:

Silver Supporter:

Sponsored by:

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Authors and Reviewers Login

Click here to access the submission and peer-review system.

Paper Submission

The ATS Program Committee invites **original, unpublished paper submissions** for ATS 2014. Paper submissions should be complete manuscripts, up to six pages (inclusive of figures, tables, and bibliography) in a standard IEEE two-column format. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status.

The complete paper must be uploaded before ~~May 16, 2014~~ May 23(extended).

Authors will be notified of the disposition of their papers by Aug.04, 2014. A submission will be considered as evidence that, upon acceptance, the author(s) will present the paper at the symposium, and will submit a final camera-ready version of the paper for inclusion in the proceedings.

For formal paper submission related information, please contact the **Program Chair**:

Yinhe Han

Institute of Computing Technology, Chinese Academy of Sciences

yinhes@ict.ac.cn

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ATS Doctoral Thesis Award(PDF)

16-19 November 2014, Hangzhou, China

Semi-Final of 2015 TTTC's E. J. McCluskey Doctoral Thesis Award

The 2014 Asian Test Symposium (ATS) doctoral thesis award is one of the semi-finals of the 2015 TTTC's E. J. McCluskey Doctoral Thesis Award. Named after Prof. E. J. McCluskey, a key contributor to the field of test technology, the TTTC's doctoral thesis award serves the purpose to promote the most impactful doctoral student work, to provide the students with the exposure to the community and the prospective employers, and to support interaction between academia and industry in the field of test technology.

For the 2015 TTTC's doctoral thesis award, semi-finals will be held (to be confirmed) at the Asian Test Symposium (ATS), the VLSI Test Symposium (VTS), the European Test Symposium(ETS), and the Latin American Test Workshop (LATW). At each semi-final, a jury will determine the winner, and the semi-final winners will compete against each other in the final, held at the 2015 International Test Conference (ITC).TTTC's E. J. McCluskey Doctoral Thesis Award will be given to the winning student and his or her advisor.

Eligibility

- Doctoral students working on test-related topics are eligible for the award.
- An individual can only participate in the contest once in a lifetime.
- Students who graduated in 2014 or will graduate in 2015 are invited.
- Participation is encouraged when the thesis is close to completion.
- Submissions to multiple regional sites are prohibited.

Submission

Contestants must submit (1) a one-page summary of their thesis (with one additional page allowed for figures and references only), (2) a separate cover page with the student's thesis title, name, affiliation, one advisor, and expected date of graduation, and (3) an endorsement by the advisor, i.e., a signed statement that he or she supports the student's participation in the contest. All submissions should be in pdf format. Submissions will undergo a selection process. Qualified contestants will be given a short presentation slot (about 7 minutes) in a designated session in 2014 ATS. The winner will be determined by the jury and announced during ATS 2014. Submission is done by email to Jiun-Lang Huang (jlhuang@ntu.edu.tw).

Key Dates

Submission deadline: August 20, 2014

Notification of qualification:September 15, 2014

Further Information

TTTC:Click here

ATS 2014: Click here

Organizer:Jiun-Lang Huang (jlhuang@ntu.edu.tw)

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On-site Registration

Accommodation for pre-conference check-in

Work time: 12pm-6pm Nov. 15

Please find the ATS'14 Registration/Accommodation desk in the lobby of Jinxi Hotel. The faculties will help you to arrange your hotel room, make payment for the room charge, and get the hotel receipt.

Note: If ATS'14 attendees want to check-in the hotel before 12pm Nov. 15, please go to the Front Desk of hotel for check-in. Your payment for the room charge should be paid after 12p.m., Nov. 15 at the ATS'14 Registration/Accommodation desk, or when you do on-site registration in Nov. 16 at the ATS'14 Registration/Accommodation desk.

On-site registration at ATS'14 Registration/Accommodation desk

Work time: 8am-9pm Nov. 16, 8am-6pm Nov. 17, 8am-6pm Nov. 18.

Please find the ATS'14 Registration/Accommodation desk in the lobby of Jinxi Hotel. The faculties will prepare the materials for your registration, help you to arrange your hotel room, make payment for the room charge, and get the hotel receipt.

On-site registration at the ATS Office Room

Work time: after 6pm of Nov.15, Nov. 17-18.

Please visit the ATS Office Room if you come after 5pm Nov. 17. The room number of ATS Office Room will be shown at the ATS'14 Registration/Accommodation desk in the lobby of Jinxi Hotel.

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Accepted Papers

Paper ID	Title
6	A Novel Circuit for Transition-Edge Detection
7	Improving Output Compaction Efficiency with High Observability Scan Chains
9	Silicon Evaluation of Cell-Aware ATPG Tests and Small Delay Tests
10	High-Speed Serial Embedded Deterministic Test for System-on-Chip Designs
11	Circuit Parameter Independent Test Pattern Generation for Interconnect Open Defects
12	Reliability-Driven Pipelined Scan-Like Testing of Digital Microfluidic Biochips
13	Design of a Radiation Hardened Latch for Low-power Circuits
14	On-Line Transition-Time Monitoring for Die-to-Die Interconnects in 3D ICs
16	An On-Line Timing Error Detection Method for Silicon Debug
18	On-chip implementation of an integrator-based servo-loop for ADC static linearity test
19	Parallel Path Delay Fault Simulation for Multi/Many-Core Processors with SIMD Units
21	BIST-Assisted Tuning Scheme for Minimizing IO-Channel Power of TSV-Based 3D DRAMs
23	On-line Path Delay Sensor for Environments with large Temperature Fluctuations
25	Low Power Test Compression with Programmable Broadcast-based Control
26	Exploit Dynamic Voltage and Frequency Scaling for SoC Test Scheduling under Thermal Constraints
27	Temperature and Voltage Estimation Using Ring-Oscillator-Based Monitor for Field Test
30	Dual-Purpose Mixed-Level Test Generation Using Swarm Intelligence
33	Two-Step Dynamic Encoding for Linear Decompressors
34	Dual-Speed TAM Optimization of 3D SoCs for Mid-Bond and Post-Bond Testing

37	Timing Evaluation Tests for Scan Enable Signals with Application to TDF Testing
42	A Resizing Method to Minimize Effects of Hardware Trojans
43	Optimal Redundancy Designs for CNFET-Based Circuits
46	A Scalable and Parallel Test Access Strategy for NoC-based Multicore System
49	Testing of Non-Volatile Logic-Based System Chips
50	On Covering Structural Defects in NoCs by Functional Tests
51	Testability-Driven Fault Sampling for Deterministic Test Coverage Estimation of Large Designs
53	High Quality Testing of Grid Style Power Gating
58	An Efficient Diagnosis Pattern Generation Procedure to Distinguish Stuck-at Faults and Bridging Faults
60	Built-In Scrambling Analysis for Yield Enhancement of Embedded Memories
61	Intra-Channel Reconfigurable Interface for TSV and Micro Bump Fault Tolerance in 3-D RAMs
64	FPGA-Based Subset Sum Delay Lines
68	Diagnosing Cell Internal Defects Using Analog Simulation-based Fault Models
69	Methodology for Early RTL Testability and Coverage Analysis and its Application to Industrial Designs
70	Generator for Test Set Construction of SMGF in Reversible Circuit by Boolean difference method
73	An All Digital Distributed Sensor Network Based Framework for Continuous Noise Monitoring and Timing Failure Analysis in SoCs
74	High Resolution Pulse Propagation Driven Trojan Detection In Digital Logic:Optimization Algorithms and Infrastructure
75	On the Generation of Diagnostic Test Set for Intra-Cell Defects
76	On Supporting Sequential Constraints for On-Chip Generation of Post-Silicon Validation Stimuli
77	Physically Aware Diagnostic Resolution
79	Predicting IC Defect Level using Diagnosis
80	A Case Study on Implementing Compressed DFT Architecture
84	SRAM array yield estimation under spatially-correlated process variation
89	A Cost-Effective Stimulus Generator for Battery Channel Characterization in Electric Vehicles
91	Optimized Pre-bond Test Methodology for Silicon Interposer Testing
92	An ATE Based 32 Gbaud PAM-4 At-Speed Characterization and Testing Solution
94	A Heuristically Mechanical Model for Accurate and Fast Soft Error Analysis

Conference Admin

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NEWS

2014/11/06	**On-site Registration**
2014/08/26	Registration System online.
2014/08/09	Accepted Papers.
2014/05/07	ATS Doctoral Thesis Award.
2014/05/04	Submission system is opened.
2014/04/24	ATS Best Paper Award.

Important Deadlines

Submission deadline:	~~May. 23,2014~~
Notification of acceptance:	~~Aug. 10, 2014~~
Camera ready manuscript:	~~Sept. 05, 2014~~

Sponsors

IEEE Computer Society

Test Technology Technical Council

Institute of Computing Technology

Best Paper Award: ATS'14 will present a Best Paper Award to a selected paper of exceptional quality. The evaluation will be conducted by an award committee constituted by experts covering all aspects of test technology, based on the criteria of innovation, potential impact, and presentation quality.

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In cooperation with Zhejiang A & F University, China

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ATS'14 国内作者注册

ATS会议注册费用	在2014年10月24号之前(RMB)	在2014年10月24号之后(RMB)
IEEE 会员*1,	3,200.00	3,900.00
非IEEE 会员*1,	3,900.00	4,600.00
IEEE 学生会员*2	1,800.00	2,100.00
非会员学生*2	3,200.00	3,900.00
IEEE 终生会员	1,800.00	2,100.00
ATS录用论文额外页数*3	每页950.00	
ATS Social Event票*4	500.00	

Tutorial注册费用*5	在2014年10月24号之前(RMB)	在2014年10月24号之后(RMB)
IEEE 会员	800.00	1,000.00
非正式会员	1,000.00	1,200.00
学生	500.00	600.00

*1 IEEE会员和非会员的注册费包括了会议费用，午餐票，Social Event。

*2 学生费用不包括Social Event，可在会场现场购买。

*3 每篇论文超过6页的额外页数费用必须在2014年9月15日前支付。请在上面注明论文的ID。每篇录用论文最多可申请2页额外页。

*4 Social Event包括旅行参观和宴会（安排在11月18日下午和晚上）。

*5 此价格为国内代表六五折优惠价格（由中国计算机学会容错计算专委会给国内代表补贴），包含11月16日的2个Tutorials。

** 注意：如果作者在2014年9月15日前没有注册，录用的论文会在没有提醒的情况下取消。

请下载并填写附件中表格，按照表格中支付方式支付款项之后发电子邮件/邮寄附件到:

Tiancheng Wang (王天成)，ATS 2014 Registration Chair

电子邮箱: ats14@ict.ac.cn ;

邮寄地址: 北京市海淀区科学院南路6号 中科院计算所体系结构国家重点实验室

王天成 收， 邮政编码：**100190**

如果有任何问题，请联系ats14@ict.ac.cn.

ATS 2014 Advance Program

Nov. 16

- **8:30am – 12:00pm**
  Tutorial I: Test, Diagnosis, and Root-Cause Identification of Failures for Boards and Systems
  Prof. Krishnendu Chakrabarty, Duke University

- **2:00pm-6:00pm**
  Tutorial II: Statistical Adaptive Test Methods Targeting 'Zero Defect' IC Quality and Reliability
  Prof. Adit D. Singh, Auburn University

Nov. 17

- **8:30am – 9:00am**
  Opening Session
- **9:00am – 10:00am**
  Keynote: Improving Design, Manufacturing, and Even Test through Test-Data Mining
  Prof. Shawn Blanton, Carnegie Mellon University
- **10:00am – 10:30am Coffee break**
- **10:30am – 11:15am**
  Invited talk I: Transformation of DFT: From Load Board to Dashboard
  Mr. Greg Aldrich, Marketing Director at Mentor Graphics
- **11:15am – 12:00pm**
- **Invited talk II: The Characterization Challenges in Modeling Semi-Floating Gate Transistors**
  Prof. David Wei Zhang, Fudan University

- **12:00pm – 1:30pm Lunch**

- **1:30pm – 2:45pm Session 1A/1B/1C**

Session 1A: 3D Testing

Session Chair: Li Jiang, Shanghai Jiao Tong University

- **BIST-Assisted Tuning Scheme for Minimizing IO-Channel Power of TSV-Based 3D DRAMs**

Yun-Chao Yu[1], Chi-Chun Yang[1], Jin-Fu Li[1], Chih-Yen Lo[2], Chao-Hsun Chen[2], Jenn-Shiang Lai[2], Ding-Ming Kwai[2], Yung-Fa Chou[2], and Cheng-Wen Wu[3]

[1]Department of Electrical Engineering National Central University

[2]Information and Communication Research Lab. Industrial Technology Research Institute

[3]Department of Electrical Engineering, National Tsing Hua University

- **Dual-Speed TAM Optimization of 3D SoCs for Mid-Bond and Post-Bond Testing**

Kele Shen[1], Dong Xiang[2] and Zhou Jiang[2]

[1]Department of Computer Science, Tsinghua University

[2]School of Software, Tsinghua University

- **Optimized Pre-bond Test Methodology for Silicon Interposer Testing**

Katherine Shu-Min Li[1], Sying-Jyan Wang[2], Jia-Lin Wu[1], Cheng-You Ho[1], Yingchieh Ho[3], Ruei-Ting Gu[1,4], Bo-Chuan Cheng[4]

[1]Department of Computer Science, National Sun Yat-sen University, Kaohsiung, Taiwan

[2]Department of Computer Science, National Chung Hsing University, Taichung, Taiwan

[3]Department of Electrical Engineering, National Dong Hwa University, Hualien, Taiwan

[4]Advanced Semiconductor Engineering (ASE) Group, Kaohsiung, Taiwan

Session 1B: Reliability

Session Chair: Zhiyuan Wang, Huawei Crop.

- **Design of a Radiation Hardened Latch for Low-power Circuits**

Huaguo Liang[1], Zhi Wang[1], Zhengfeng Huang[1], and Aibin Yan[2]

[1]School of Electronic Science and Applied Physics, Hefei University of Technology, Hefei 230009, P.R. China

[2]School of Computer and Information, Hefei University of Technology, Hefei 230009, P.R. China

- **Optimal Redundancy Designs for CNFET-Based Circuits**

Da Cheng, Fangzhou Wang, Feng Gao, and Sandeep K. Gupta

Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles, CA, USA

- **A Heuristically Mechanical Model for Accurate and Fast Soft Error Analysis**

Jiajia Jiao, Yuzhuo Fu

School of Micro Electronics, Shanghai Jiao Tong University, Shanghai, China

Special Session 1C: Resilient Circuit Design and Test

Moderator: Mehdi Tahoori, Karlsruhe Institute of Technology, Germany

- **Error Resilient Real-Time State Variable Systems for Signal Processing and Control**

  Suvadeep Banerjee[1], A´ lvaro Go´mez-Pau[2], Abhijit Chatterjee[1] and Jacob A. Abraham[3]

  [1]School of Electrical and Computer Engineering, Georgia Institute of Technology

  [2]Universitat Polit`ecnica de Catalunya, Barcelona, Spain

  [3]Electrical and Computer Engineering, University of Texas at Austin

- **Variability and Soft-Error Resilience in Dependable VLSI Platform**

  Yukio Mitsuyama[1] , and Hidetoshi Onodera[2],

  [1]Kochi University of Technology, [2] Kyoto University

- **Adaptive Mitigation of Parameter Variations**

  Farshad Firouzi[1], Fangming Ye[2], Saman Kiamehr[1], Krishnendu Chakrabartyz[2], and Mehdi B. Tahooriy[1]

  [1]Karlsruhe Institute of Technology, Germany

  [2]Department of Electrical and Computer Engineering, Duke University, Durham, NC, USA

- **2:45pm – 3:15pm Coffee break**

- **3:15pm – 4:30pm Session 2A/2B/2C**

Session 2A: Testing of Emerging Technologies

Session Chair: Sandeep Gupta, Univ. of Southern California

- **Reliability-Driven Pipelined Scan-Like Testing of Digital Microfluidic Biochips**

  Zipeng Li[1], Trung Anh Dinh[2], Tsung-Yi Ho[3], Krishnendu Chakrabarty[1]

  [1]Department of Electrical and Computer Engineering, Duke University, Durham, NC, USA

  [2]Graduate School of Information Science and Engineering, Ritsumeikan University, Shiga, Japan

  [3]Computer Science Department, National Chiao Tung University, Hsinchu, Taiwan

- **A Cost-Effective Stimulus Generator for Battery Channel Characterization in Electric Vehicles**

  Shao-Feng Hung, Long-Yi Lin, and Hao-Chiao Hong

  Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan

- **Generator for Test Set Construction of SMGF in Reversible Circuit by Boolean Difference Method**

  Bappaditya Mondal[1], Dipak Kumar Kole[1], Debesh Kumar Das[2] and Hafizur Rahaman[1]

  [1]Department of Information Technology, Indian Institute of Engineering Science and Technology, Shibpur, India

  [2]Department of Computer Science and Engineering, Jadavpur University, Kolkata, India

Session 2B: SoC Testing

Session Chair: Yu Huang, Mentor Graphics

- **High-Speed Serial Embedded Deterministic Test for System-on-Chip Designs**

  Maciej Trawka Grzegorz Mrugalski[1], Nilanjan Mukherjee[1], Artur Pogiel[2], Janusz Rajski[2]

  Jakub Janicki[3], Jerzy Tyszer[3]

  [1]Gdańsk University of Technology, 80-233 Gdańsk, Poland

  [2]Mentor Graphics Corporation, Wilsonville, OR 97070, USA

  [3]Poznań University of Technology, 60-965 Poznań, Poland

- **A Scalable and Parallel Test Access Strategy for NoC-Based Multicore System**

  Taewoo Han, Inhyuk Choi, Hyunggoy Oh, Sungho Kang

  Department of Electrical and Electronic Engineering, Computer systems & reliable SoC Lab., Yonsei University, Seoul, Korea

- **On Covering Structural Defects in NoCs by Functional Tests**

  Atefe Dalirsani, Nadereh Hatami, Michael E. Imhof, Marcus Eggenberger, Gert Schley,

  Martin Radetzki, Hans-Joachim Wunderlich

  Institute of Computer Architecture and Computer Engineering, University of Stuttgart, Germany

Special Session 2C: Design, Verification and Application of IEEE 1687

Moderator: Erik Larsson, Lund University, Sweden

- **Design, Verification and Application of IEEE 1687**

  Farrokh Ghani Zadegan[1], Erik Larsson[1], Artur Jutman[2], Sergei Devadze[2], Rene´ Krenz-Baath[3]

  [1]Lund University, Lund, Sweden

  [2]Testonica Lab, Tallinn, Estonia

  [3]Hochschule Hamm-Lippstadt, Hamm, Germany

- **4:30pm – 5:00pm Coffee break**

- **5:00pm – 6:40pm Session 3A/3B/3C**

Session 3A: Post-Silicon Validation

Session Chair: Michael Hsiao, Virginia Tech.

- **Silicon Evaluation of Cell-Aware ATPG Tests and Small Delay Tests**

  Fan Yang[1], Sreejit Chakravarty[1], Arun Gunda[1], Nicole Wu[2] and Jianyu Ning[2]

  [1]Avago Technologies, San Jose, CA, USA

  [2]Avago Technologies, Shanghai, China

- **On Supporting Sequential Constraints for On-Chip Generation of Post-Silicon Validation Stimuli**

  Xiaobing Shi and Nicola Nicolici

  Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada

- **Predicting IC Defect Level using Diagnosis**

  Cheng Xue and R.D. (Shawn) Blanton

  ECE Department, Carnegie Mellon University, Pittsburgh, PA, USA

Session 3B: Testability and Test Generation

Session Chair: Hans-Joachim Wunderlich, University of Stuttgart

- **Testability-Driven Fault Sampling for Deterministic Test Coverage Estimation of Large Designs**

Kun-Han Tsai

Mentor Graphics Corporation, Wilsonville, OR 97070, USA

- **Methodology for Early RTL Testability and Coverage Analysis and Its Application to Industrial Designs**

  Chandan Kumar[1], Fadi Maamari[1], Kiran Vittal[1], Wilson Pradeep[2], Rajesh Tiwari[2], Srivaths Ravi[2]

  [1]Atrenta Inc., San Jose, U.S.A

  [2]Texas Instruments Inc., Bengaluru, India

- **Circuit Parameter Independent Test Pattern Generation for Interconnect Open Defects**

  Dominik Erb[1], Karsten Scheibler[1], Matthias Sauer[1], Sudhakar M. Reddy[2], Bernd Becker[1]

  [1]Chair of Computer Architecture, University of Freiburg, Germany

  [2]Dept. of ECE, University of Iowa, USA

Session 3C: TTTC's Doctoral Thesis Award: Asian Semi-Final

Session Chair: Jiun-Lang Huang, National Taiwan University

- **Researching on the critical techniques of metamorphic testing to provide more effective test oracle**

  Zhan-Wei Hui,

  PLA Univ. of Science and Technology

- **Yield and reliability enhancement for 3D ICs**

  Li Jiang,

  The Chinese University of Hong Kong

- **An analytical model driven framework for accurate and efficient soft error analysis in processors**

  Jiajia Jiao,

  Shanghai Jiao Tong University

- **Diagnosis techniques for identifying faults in digital VLSI system**

  Subhadip Kundu,

  IIT Kharagpur

- **Multiple-fault-oriented fault diagnosis for digital integrated circuits**

Jing Ye,

Institute of Computing Technology, Chinese Academy of Sciences

Nov. 18

- **9:00am – 10:15am Session 4A/4B/4C**

Session 4A: Yield Optimization of Memory

Session Chair: Jin-Fu Li, National Central University

- **Built-In Scrambling Analysis for Yield Enhancement of Embedded Memories**

  Shyue-Kung Lu[1], Hao-Cheng Jheng[1], Hao-Wei Lin[1], Masaki Hashizume[2], and Seiji Kajihara[3]

  [1]Dept. Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan

  [2] Institute of Technology and Science, The University of Tokushima, Tokushima, Japan

  [3]Dept. Creative Informatics, Kyushu Institute of Technology, Kyushu, Japan

- **Intra-Channel Reconfigurable Interface for TSV and Micro Bump Fault Tolerance in 3-D RAMs**

  Kuan-Te Wu[1], Jin-Fu Li[1], Yun-Chao Yu[1], Chih-Sheng Hou[1], and Chi-Chun Yang[1], Ding-Ming Kwai[2], Yung-Fa Chou[2] and Chih-Yen Lo[2]

  [1]Department of Electrical Engineering, National Central University, Taoyuan, Taiwan 320

  [2]Information and Communication Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan 310

- **SRAM array yield Estimation under spatially-correlated process variation**

  Jizhe Zhang and Sandeep Gupta

  Department of Electrical Engineering, University of Southern California

Session 4B: On-Line Parameter Testing

Session Chair: Xiaoxiao Wang, Beihang University

- **Temperature and Voltage Estimation Using Ring-Oscillator-Based Monitor for Field Test**

  Yousuke Miyake[1], Yasuo Sato[1], Seiji Kajihara[1]and YukiyaMiura[2]

  [1]Kyushu Institute of Technology, Iizuka, Japan

[2]*Tokyo Metropolitan University, Tokyo, Japan*

- **On-Line Transition-Time Monitoring for Die-to-Die Interconnects in 3D ICs**

  Shi-Yu Huang[1], Hua-Xuan Li[1], Zeng-Fu Zeng[1], Kun-Han Tsai[2], and Wu-Tung Cheng[2]

  [1]*Electrical Engineering Department, National Tsing Hua University, Taiwan*

  [2]*Silicon Test Solutions, Mentor Graphics*

- **A Novel Circuit for Transition-Edge Detection: Using a Stochastic Comparator Group to Test Transition-Edge**

  Takahiro J. Yamaguchi[1,3], James S. Tandon[2,3], Satoshi Komatsu[3,4], Kunihiro Asada[3]

  [1]*Advantest Laboratories, Ltd., Sendai, Miyagi, Japan*

  [2]*Microsemi, San Jose, CA, USA*

  [3]*D2T, VDEC, The University of Tokyo, Tokyo, Japan*

  [4]*School of Engineering, Tokyo Denki University, Tokyo, Japan*

Session 4C: Embedded Tutorial-Hierarchical Scan Compression 1

Yu Huang, Mentor Graphics

ZhenXin Sun, Cadence

Ang Li, Synopsys

- **10:15am – 10:45am Coffee break**

- **10:45am – 12:00pm Session 5A/5B/5C**

Session 5A: Power/Temperature-Aware Testing

Session Chair: Seiji Kajihara, Kyushu Institute of Technology

- **Low Power Test Compression with Programmable Broadcast-Based Control**

  Sylwester Milewski[1], Grzegorz Mrugalski[2], Janusz Rajski[2], Jerzy Tyszer[1]

  [1]*Poznań University of Technology, 60-965 Poznań, Poland*

  [2]*Mentor Graphics Corporation, Wilsonville, OR 97070, USA*

- **Exploit Dynamic Voltage and Frequency Scaling for SoC Test Scheduling under Thermal Constraints**

  Li Ling, Jianhui Jiang

School of Software Engineering, Tongji University, Shanghai, China

- **High Quality Testing of Grid Style Power Gating**

  Vasileios Tenentes[1], Saqib Khursheed[2], Bashir M. Al-Hashimi[1], Shida Zhong[1], Sheng Yang[1]

  [1]ECS, University of Southampton, UK.

  [2]Electrical Engineering & Electronics, University of Liverpool, UK.

Session 5B: Trojan/Fault Detection with High Resolution

Session Chair: Katherine Shu-Min Li, National Sun Yat-Sen University

- **A Resizing Method to Minimize Effects of Hardware Trojans**

  Byeongju Cha and Sandeep K. Gupta

  Ming Hsieh Department of Electrical Engineering, University of Southern California Los Angeles, USA

- **High Resolution Pulse Propagation Driven Trojan Detection In Digital Logic: Optimization Algorithms and Infrastructure**

  Sabyasachi Deyati[1] ,Barry John Muldrey[1], Adit Singh[2], Abhijit Chatterjee[1]

  [1]Electrical & Computer Engineering, Georgia Institute of Technology, Atlanta GA 30332, USA

  [2]Department of Electrical Engineering, Auburn University, AL 36849, USA

- **Physically-Aware Diagnostic Resolution**

  John A. Porche, R. D. (Shawn) Blanton

  Dept. of ECE Carnegie Mellon University Pittsburgh, PA 15213

Session 5C: Embedded Tutorial- Hierarchical Scan Compression 2

Yu Huang, Mentor Graphics

ZhenXin Sun, Cadence

Ang Li, Synopsys

- **12:00pm – 1:30pm Lunch**
- **1:30pm – 3:10pm Session 6A/6B/6C**

Session 6A: Analog/Memory Testing

Session Chair: Jiun-Lang Huang, National Taiwan University

- **On-chip implementation of an Integrator-Based servo-loop for ADC static linearity test**

  Guillaume Renaud[1], Manuel J. Barragan[1], and Salvador Mir[1], Marc Sabut[2]

  [1]Universite Grenoble Alpes, TIMA, F-38000 Grenoble, France ´ CNRS, TIMA, F-38000 Grenoble, France

  [2]STMicroelectronics Grenoble 12, Rue Jules Horowitz, F-38000 Grenoble, France

- **An ATE Based 32 Gbaud PAM-4 At-Speed Characterization and Testing Solution**

  Jose Moreira[1], Hubert Werkmann[1], Masahiro Ishida[1], Bernhard Roth[1], Volker Filsinger[2], Sui-Xia Yang[1]

  [1]Advantest

  [2]SHF Communication Technologies

- **Testing of Non-Volatile Logic-Based System Chips**

  Yong-Xiao Chen and Jin-Fu Li

  Advanced Reliable Systems (ARES) Lab, Department of Electrical Engineering, National Central University, Jhongli, Taiwan 320

- **Dual-Purpose Mixed-Level Test Generation Using Swarm Intelligence**

  Kelson Gent and Michael S. Hsiao

  Bradley Department of Electrical and Computer Engineering Virginia Tech, Blacksburg, VA 24061, USA

Panel Session 6B: Big Data for Test

Moderators: K.-T. Tim Cheng, University of California, Santa Barbara
Harry H. Chen, MediaTek Inc.

- **Learning from Production Test Data: Correlation Exploration and Feature Engineering**

  Fan Lin, Chun-Kai Hsu, and Kwang-Ting Cheng

  Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106

- **Leveraging Big Data Analytics to Drive Failure Analysis in Manufacturing Operations**

  David Park,

Optimal+

- **Data Driven Design Centric Yield Learning**

  John Kim,

  Synopsys

- **Perspectives on Test Data Mining from Industrial Experience**

  Harry H. Chen,

  Design Technology Department, MediaTek Inc. Hsinchu, Taiwan

Special Session 6C: In-Field Techniques for Performance Adaption, Test, and Power-Noise Diagnosis

Moderator: Xiaoqing Wen, Kyushu Institute of Technology, Japan

- **Opportunities and Verification Challenges of Run-time Performance Adaptation**

  Masanori Hashimoto

  Dept. Information Systems Engineering, Osaka University

- **An On-Chip Digital Environment Monitor for Field Test**

  Seiji Kajihara, Yousuke Miyake, Yasuo Sato, Yukiya Miura(

  Kyushu Institute of Technology

- **On-Chip Monitoring for In-Place Diagnosis of Undesired Power Domain Problems in IC Chips**

  Makoto Nagata, Daisuke Fujimoto, Noriyuki Miura

  Graduate School of System Informatics, Kobe University, Japan

- **3:30pm – 10:00pm Social Event & Banquet**

Nov. 19

- **9:00am – 10:15am Session 7A/7B/7C**

Session 7A: Timing Variation Detection

Session Chair: Shi-Yu Huang, National Tsinghua University

- **An On-Line Timing Error Detection Method for Silicon Debug**

  Yun Cheng[1,2], Huawei Li[1], Xiaowei Li[1]

  [1]State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

  [2]University of Chinese Academy of Sciences, Beijing, China

- **An All Digital Distributed Sensor Network Based Framework for Continuous Noise Monitoring and Timing Failure Analysis in SoCs**

  Mehdi Sadi [1], Zoe Conroy [2], Bill Eklow [2], Matthias Kamm [2], Nematollah Bidokhti [2] and Mark (Mohammad) Tehranipoor [1]

  [1]Dept. of Electrical & Computer Engineering, University of Connecticut, Storrs, USA

  [2]Cisco Systems, San Jose, CA, USA

- **On-Chip Delay Sensor for Environments with large Temperature Fluctuations**

  Jibing Qiu, Guihai Yan, Xiaowei Li

  State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China

Session 7B: Delay Testing

Session Chair: Bernd Becker, University of Freiburg

- **Timing Evaluation Tests for Scan Enable Signals with Application to TDF Testing**

  Jie Zou, Chao Han and Adit D. Singh

  Department of Electrical and Computer Engineering, Auburn University, Auburn AL, 36849

- **FPGA-Based Subset Sum Delay Lines**

  Chung-Yun Wang[1], Yu-Yi Chen[1], Jiun-Lang Huang[1], Xuan-Lun Huang[2]

  [1]Graduate Institute of Electronics Engineering, Department of Electrical Engineering, National Taiwan University

  [2]Industrial Technology Research Institute, Hsinchu, Taiwan

- **Parallel Path Delay Fault Simulation for Multi/Many-Core Processors with SIMD Units**

  Yussuf Ali[1] Yuta Yamato[1] Tomokazu Yoneda[1] Kazumi Hatayama[2] Michiko Inoue[1]

  [1] Nara Institute of Science and Technology, Nara, Japan

  [2]Gunma University, Gunma, Japan

Special Session 7C: High Quality System Level Test and Diagnosis

Moderator: Hans-Joachim Wunderlich, University of Stuttgart

- **High Quality System Level Test and Diagnosis**

  Artur Jutman[1], Matteo Sonza Reorda[2], Hans-Joachim Wunderlich[3]

  [1]Testonica Lab, Tallinn, Estonia, [2]Politecnico di Torino, Italy, [3]University of Stuttgart, Germany

- **10:15am – 10:45am Coffee break**

- **10:45am – 12:00pm Session 8A/8B/8C**

Session 8A: Diagnosis

Session Chair: Sybille Hellebrand, University of Paderborn

- **An Efficient Diagnosis Pattern Generation Procedure to Distinguish Stuck-at Faults and Bridging Faults**

  Cheng-Hung Wu and Kuen-Jong Lee

  Dept. of EE, National Cheng Kung University, Taiwan

- **On the Generation of Diagnostic Test Set for Intra-cell Defects**

  Z. Sun[1], A. Bosio[1], L. Dilillo[1], P. Girard[1], A. Virazel[1], E. Auvray[2]

  [1]LIRMM UM2-CNRS, Montpellier, France

  [2]ST Microelectronics, Grenoble, France

- **Diagnosing Cell Internal Defects Using Analog Simulation-based Fault Models**

  Huaxing Tang[1], Brady Benware[1], Michael Reese[2], Joseph Caroselli[2], Thomas Herrmann[3], Friedrich Hapke[4], Robert Tao[2], Wu-Tung Cheng[1], Manish Sharma[1]

  [1]Mentor Graphics, Wilsonville, Oregon, USA

  [2]AMD, Inc. Austin, Texas, USA

  [3]GLOBALFOUNDRIES, Dresden, Germany

  [4]Mentor Graphics, Hamburg, Germany

Session 8B: Test Compression

Session Chair: Huaguo Liang, Hefei University of Technology

- **Improving Output Compaction Efficiency with High Observability Scan Chains**

  Sying-Jyan Wang[1], Che-Wei Kao[1], Katherine Shu-Min Li[2]

  [1]Department of Computer Science and Engineering, National Chung Hsing University, Taichung, Taiwan

  [2]Department of Computer Science and Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan

- **Two-Step Dynamic Encoding for Linear Decompressors**

  Emil Gizdarski

  Synopsys Inc., 700 East Middlefield Road, Mountain View, CA 94043

- **A Case Study on Implementing Compressed DFT Architecture**

  A. Chandra, S. Chebiyam, and R. Kapur

  Synopsys, Inc., 700 E. Middlefield Rd., Mountain View, CA, 94043, USA

Special Session 8C: Hardware Security

Moderator: Yier Jin, University of Central Florida

- **Leveraging Emerging Technology for Hardware Security - Case Study on Silicon Nanowire FETs and Graphene SymFETs**

  Yu Bi[1], Pierre-Emmanuel Gaillardon[2], X. Sharon Huz[3], Michael Niemierz[3], Jiann-Shiun Yuan[1], and Yier Jin[1]

  [1]Department of Electrical Engineering and Computer Science, University of Central Florida

  [2]Ecole Polytechnique F ´ ed´ erale de Lausanne (EPFL) - Switzerland ´

  [3]Department of Computer Science and Engineering, University of Notre Dame

- **Advanced Analysis of Cell Stability for Reliable SRAM PUFs**

  Alison Hosey, Md. Tauhidur Rahman, Kan Xiao, Domenic Forte, and Mohammad Tehranipoor

  ECE Department, University of Connecticut

- **On the Use of Scan Chain to Improve Physical Attacks**

  Junfeng Fan[1], Hua Xie[2], Yiwei Zhang[2]

  [1]Nationz technologies and Open Security Research, Shenzhen, China

  [2]Nationz technologies, Shenzhen, China

The 23rd Asian Test Symposium (ATS'14)

Hangzhou, China, Nov.16-19, 2014

http://ats2014.ict.ac.cn

Call for Papers

The Asian Test Symposium (ATS) provides an open forum for researchers and industrial practitioners from all countries of the world, especially from Asia, to exchange innovative ideas on system, board, and device testing with design, manufacturing and field consideration in mind.

Scope

Original papers on, but not limited to, the following areas are invited.

- Automatic Test Pattern Generation
- Fault Modeling and Simulation
- Design Verification and Validation
- Diagnosis and Debug
- Board and System Test
- Analog/Mixed-Signal Test
- High-Speed I/O Test
- RF Test
- Delay and Performance Test
- Memory Test/FPGA Test
- System-in-Package/3D Test
- Software Testing
- Hardware Security
- Boundary Scan Test
- Built-In Self-Test
- Design-for-Testability
- Test Compression
- On-Line Test
- Temperature/Power-Aware Testing
- Defect-Based Testing
- Fault Tolerance
- Dependable System
- Yield Analysis and Enhancement
- Test Quality
- Economics of Test

Submissions

Regular Sessions: The ATS'14 Program Committee invites original, unpublished paper submissions on the above topics. Paper submissions should be complete manuscripts, not exceeding six pages (including figures, tables, and bibliography) in a standard IEEE two-column format. The submission will be considered evidence that upon acceptance the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication.

ATS'14 will present a Best Paper Award to a selected paper of exceptional quality. The evaluation will be conducted by an award committee constituted by experts covering all aspects of test technology, based on the criteria of innovation, potential impact, and presentation quality.

Key Dates

- Submission deadline: ***May 16, 2014***
- Notification of acceptance: ***Aug. 4, 2014***
- Camera ready manuscript: ***Sept. 5, 2014***

Further Information

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ATS Doctoral Thesis Award

16-19 November 2014, Hangzhou, China

Semi-Final of 2015 TTTC's E. J. McCluskey Doctoral Thesis Award

The 2014 Asian Test Symposium (ATS) doctoral thesis award is one of the semi-finals of the 2015 TTTC's E. J. McCluskey Doctoral Thesis Award. Named after Prof. E. J. McCluskey, a key contributor to the field of test technology, the TTTC's doctoral thesis award serves the purpose to promote the most impactful doctoral student work, to provide the students with the exposure to the community and the prospective employers, and to support interaction between academia and industry in the field of test technology.

For the 2015 TTTC's doctoral thesis award, semi-finals will be held (to be confirmed) at the Asian Test Symposium (ATS), the VLSI Test Symposium (VTS), the European Test Symposium (ETS), and the Latin American Test Workshop (LATW). At each semi-final, a jury will determine the winner, and the semi-final winners will compete against each other in the final, held at the 2015 International Test Conference (ITC).

TTTC's E. J. McCluskey Doctoral Thesis Award will be given to the winning student and his or her advisor.

Eligibility

- Doctoral students working on test-related topics are eligible for the award.
- An individual can only participate in the contest once in a lifetime.
- Students who graduated in 2014 or will graduate in 2015 are invited.
- Participation is encouraged when the thesis is close to completion.
- Submissions to multiple regional sites are prohibited.

Submission

Contestants must submit (1) a one-page summary of their thesis (with one additional page allowed for figures and references only), (2) a separate cover page with the student's thesis title, name, affiliation, one advisor, and expected date of graduation, and (3) an endorsement by the advisor, i.e., a signed statement that he or she supports the student's participation in the contest. All submissions should be in pdf format.

Submissions will undergo a selection process. Qualified contestants will be given a short presentation slot (about 7 minutes) in a designated session in 2014 ATS. The winner will be determined by the jury and announced during ATS 2014.

Submission is done by email to Jiun-Lang Huang (jlhuang@ntu.edu.tw).

Key Dates

- **Submission deadline:** **August 20, 2014**
- **Notification of qualification:** **September 15, 2014**

Further Information

- TTTC: www.tttc-events.org/tttc_website/index.php?section=awards_doctoral_thesis
- ATS 2014: ats2014.ict.ac.cn
- Organizer: Jiun-Lang Huang (jlhuang@ntu.edu.tw)

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