



Special Workshop in Honor of Prof. Hideo Fujiwara

November 20, 2011 (in conjunction with [ATS 2011](#))
Crowne Plaza Hotel, New Delhi, India

[Prof. Hideo Fujiwara](#)

Advances in ATPG and DFT

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Design and Test have always led an uneasy co-existence. Designers have viewed Test as encroaching on their performance and area goals, and placing unnecessary bounds on their creativity. However, rising cost of Test and increasing limitations of available tester platforms continue to place additional requirements on design. Traditional testing methods utilizing stuck-at and transition fault models are no longer adequate to achieve target quality in many designs.

Today, Testing needs to address defects and failure modes due to process, thermal and voltage variations. Complexity of test pattern development against physical fault models that account for parametric variations appear insurmountable. Reduced manufacturing tolerance due to sub-wavelength lithography, time dependent device degradation along with interplay with ambient factors such as temperature and voltage necessitates new methods merged with fault tolerant designs while continue to address the test problem.

[Prof. Hideo Fujiwara](#) over the course of his illustrious career has devoted his energies to solving problems similar to and beyond those mentioned above. His research in VLSI Testing runs the gamut from ATPG, complexity theory, and Design for Test. This workshop seeks to celebrate Prof. Fujiwara's contribution to the field of VLSI Testing, and his efforts in fostering original thinking as a dedicated educator and mentor.

The major goals of the workshop are:

- to highlight Prof. Fujiwara's significant contributions

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- to bring together Prof. Fujiwara's students, associates, friends, and fans for a memorable reunion

The symposium will feature three types of presentations:

- Invited talks from well known people in academia/industry
- Research summaries by various students and associates
- Informal talks during dinner time bringing back memories

Websites:

o **Workshop:** <http://www.serc.iisc.ernet.in/~viren/WHF/>

o **ATS:** www.ecs.umass.edu/ece/ats11/

o **WRTLTL:** www.ieee-wrtl.org

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Workshop Schedule

Special Workshop in Honour of Prof. Hideo Fujiwara

Nov 20, 2011 at Crowne Plaza Hotel, New Delhi

Advances in ATPG and DFT

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|----------------------|--|
| 10:30 am to 11:00 am | Registration Coffee |
| 11:00 am to 11:15 am | Inauguration Introduction by Virendra Singh and Adit Singh |
| 11:15 am to 11:40 am | Invited Talk 1 Speaker: Krishnendu Chakrabarty Topic: The Quest for High-Level Test Generation and DFT |
| 11:40 am to 12:05 am | Invited Talk 2 Speaker: Wen Xiaoqing Topic: A FAN (or Fun) Impact |
| 12:05 pm to 12:30 pm | Invited Talk 3 Speaker: Erik Larsson Topic: Test Planning for Core-Based System Chips |
| 12:30 pm to 2:00 pm | LUNCH |
| 2:00 pm to 2:25 pm | Invited Talk 4 Speaker: Alex Orailoglu Topic: Diagnosing Scan Chain Timing Faults through Statistical Feature Analysis of Scan Images |
| 2:25 pm to 2:50 pm | Invited Talk 5 Speaker: Debesh Das |
| 2:50 pm to 3:15 pm | Invited Talk 6 Speaker: Kewal Saluja Topic: PLA Testing: Myths and Facts |
| 3:15 pm to 3:35 pm | Talk by Prof. Hideo Fujiwara |
| 3:35 pm to 3:45 pm | Felicitations of Prof. Fujiwara |

Social Program

4:00 pm to 6:30 pm: Guided tour to [Outub Minar](#)

Buses will leave at 4:00 pm from Crowne Plaza Hotel

Banquet

6:30 pm to 8:30 pm at [Fortune Park Boulevard Resort, Chatterpur](#), New Delhi.

Informal Session: Personal experiences with Prof. Fujiwara

8:30 pm to 9:30 pm: Return to Crowne Plaza Hotel (Drive by [Red Fort](#))