WRTLT'01 The Second Workshop on RTL ATPG & DFT

November 22-23, 2001, Nara, Japan

(Naramachi-center, 38 Higashiterabayashi-cho, Nara-shi, Nara 630-8362, Japan)

Sponsored by *IEEE Computer Society Test Technology Technical Council*
In cooperation with *Technical Group on Fault Tolerant Systems, IEICE*

Website for WRTLT'02 : http://www.ip.elec.mie-u.ac.jp/~wrtlt02/

SCOPE

The Workshop on RTL ATPG & DFT (WRTLT) provides an international forum for interchanging ideas and implementation experiences on register transfer (RT) level automatic test pattern generation (ATPG) and design for testability (DFT). For systems on chip (SOC) devices, it has become a real hot topic to improve VLSI testability using high-level descriptions. Now in its 2nd year, just after the ATS'01, papers are solicited on all aspects of RT-level testing techniques. Photocopies of accepted papers will be handed out at the workshop site. We hope and expect the workshop will provide all participants with new ideas and food for thought through informal interactions and discussions.

Topics of interest include(but not limited to)

- Functional fault modeling
- RT-level ATPG
- RT-level DFT
- RT-level BIST
- Relationship between RTL and gate level testing

IMPORTANT DATES

- Submission: ~~July 31, 2001 => twelve noon, August 10, Japan Standard Time.~~
- Acceptacnce: ~~August 31, 2001~~
- Final version: ~~to be announced~~
- Registration: ~~Advance registraton due: October 20, 2001~~
  => **On-site registration**
- **Reception:** **November 21, 2001. 19:00-21:00.**
  At a restaurant, "Kissa Naramachi", 1st Floor, Naramachi Center.
  (Snack and drink will be served. Please join.)
- **Workshop:** **November 22-23, 2001**

For up-to-date information refer to this WRTLT'01 web site or contact the workshop chairs.

Final Program (Updated 11/15 2001)

WRTLT'01 Final Program (11/15 2001)

WRTLT'01 Advance Program (Updated 10/06 2001)

Registration (Updated 9/19 2001)

Advance Registration Instruciotns and **Registration Form**

Advance registration due: October 20, 2001

Access & Accommodations (Updated 11/01 2001, access to Nara)

Access

You can find an access to Nara here. If you come to Nara from Kyoto after ATS'01, we recommend to use a Kintetsu line other than a JR line. KINTETSU Kyoto station is adjacent to JR Kyoto station, and both are close to Righa Royal Hotel KYOTO (the place of ATS'01). Here is a MAP around Nara-Machi center and stations. KINTETSU Nara station is an underground station. If you go to the hotels, use the EXIT 4 and go up to the ground. If you go to Nara-Machi center, use the EXIT 2.

Accommodations

We keep some rooms for WRTLT'01 participants in Hotel Fujita NARA (English page) and NARA Washington Hotel Plaza (Japanese page). We also hold a banquet at Hotel Fujita NARA. Please use the following Hotel Reservation Form. For guaranteed reservation send the completed form by Oct. 31, 2001 to the HOTEL.

Hotel Fujita NARA (PDF, Word) (Updated 10/18 2001, Fax number was incorrect)
Nara Washington Hotel Plaza (PDF, Word)(Updated 9/18 2001)

Call for Papers

PDF version TEXT version

Organization

General Chair

Hideo Tamamoto (Akita University, Japan) tamamoto@ie.akita-u.ac.jp

Program Co-Chairs

Kazuhiko Iwasaki (Tokyo Metropolitan University, Japan) iwasaki@eei.metro-u.ac.jp
Xiaowei Li (Peking University, China) lxw@pku.edu.cn

Finance Chair

Hiroshi Yokoyama (Akita University, Japan) yokoyama@ie.akita-u.ac.jp

Local Arrangements Chair

Michiko Inoue (NAIST, Japan) kounoe@is.aist-nara.ac.jp

Program Commitee

S. Fukumoto, Japan	T. Inoue, Japan	X. Wen, USA
S. Gupta, USA	Z. Li, China	C-W. Wu, Taiwan
K. Hatayama, Japan	T. Masuzawa, Japan	S. Xu, China
T. Hayashi, Japan	K. Saluja, USA	H. Youn, Korea
T. Hosokawa, Japan	Y. Sun, China	D. Zhang, China
W. Huang, China	J. P. Teixeira, Portugal	

WRTLT Steering Committee

Chair:
Yinghua Min (Academia Sinica, China)

Members:

Hideo Fujiwara (NAIST, Japan)
Kazuhiko Iwasaki (Tokyo Metropolitan University, Japan)
Xiaowei Li (Peking University, China)
Kewal K. Saluja (University of Wisconsin, USA)
Terumine Hayashi (Mie University, Japan)
Hideo Tamamoto (Akita University, Japan)
J. Paulo Teixeira (IST/INESC, Portugal)
Dafang Zhang (Hunan University, China)
Alex Orailoglu (University of California, USA)

Links

- **Nara City Tourism Section's Home Page**
- **Nara Prefecture**
- **Nara City**
- **Naramachi-center (Japanese)**
- **ATS'01 Web site**

WRTLT'01 Final Program

Registration (Meeting room 4, Naramachi center 3F)
19:00 - 21:00 Nov. 21
8:40 - 18:00 Nov. 22
9:00 - 15:00 Nov.23

Technical Session (Meeting room 2, Naramachi center 3F)

Nov. 21, 2001

Reception
19:00 - 21:00 (Kissa Naramachi, Naramachi center 1F)

Nov. 22, 2001

Opening
9:00 - 9:15

Invited talk
9:15 - 10:00 (45-min)
Chair : K. Iwasaki
VCore Based Design Technology for the Next Generation SOC
M. Muraoka - Semiconductor Technology Academic Research Center, Japan

Session 1
10:20 - 12:00 (100-min)
Chair : K. Hatayama

1.1 : Why RTL ATPG?
Y. Min - Chinese Academy of Sciences, China
1.2 : A Scheduling Method in High-Level Synthesis for RTL Acyclic Partial Scan Design
T. Inoue, T. Miura, A. Tamura - Hiroshima City University, Japan
H. Fujiwara - Nara Institute of Science and Technology, Japan
1.3 : Modeling and Organizing of RTL Transfer Faults
Z. Yin, Y. Min, X. Li - Chinese Academy of Sciences, China
1.4 : Partial Scan Testing on the Register-Transfer Level
B. S. Greene - C-Level Design Inc., U.S.A.
S. Mourad - Santa Clara University, U.S.A.

Lunch
Steering Committee Meeting (members only)
(Meeting room 1, Naramachi center3F)
12:00 - 13:30

Session 2
13:30 - 14:45 (75-min)
Chair : T. Masuzawa

2.1 : Design for Consecutive Testability of Systems-on-a-Chip with Built-In Self Testable Cores
T. Yoneda, H. Fujiwara - Nara Institute of Science and Technology, Japan
2.2 : Memory-Based Reconfigurable Chip Architecture and Its RT-Level BIST
Y. Yamada, Y. Ichinoseki, K. Ichino, S. Fukumoto, K. Iwasaki - Tokyo Metropolitan University, Japan
M. Sato - Hitachi, Ltd., Japan
2.3 : Circular ScanBIST: A Highly Efficient BIST Technique for Sequential Circuits
K. S. Kim - Intel Corporation, U.S.A.

Session 3
15:00 - 16:15 (75-min)
Chair : S. Fukumoto

3.1 : Devising an RT-Level ATPG for uProcessor Cores
F. Corno, G. Cumani, M. Sonza Reorda, G. Squillero - Politecnico di Torino, Italy
3.2 : Constraint Driven Pin Mapping for Concurrent SOC Testing
Y. Huang, S. M. Reddy - University of Iowa, U.S.A.
N. Mukherjee, C. Tsai, O. Samman, Y. Zaidan, Y. Zhang, W. Cheng - Mentor Graphics Corporation, U.S.A.

3.3 : A DSP-based Test Scheme and Its Optimization for Systems on a Chip
H. Hu, S. Yihe - Tsinghua University, China

Session 4
16:30 - 18:00 (90-min)
Chair : K. Saluja

4.1 : Semi-Random Testing for Combinational Circuits
S. Xu, J. Chen - Shanghai University, China
4.2 : Module-based Hierarchical Test Generation for Combinational Circuits at Register-Transfer Level
X. Huang, D. Zhang, Y. Min - Human University, China
4.3 : A flexible platform for the functional validation of programmable circuits
R. Velazco, F. Faure - TIMA Laboratory, France
4.4 : Non-Scan Design for Testability for RTL Circuits Based on Conflict Analysis
D. Xiang, S. Gu - Tsinghua University, China
4.5 : An FSM-Based Programmable Memory BIST Architecture
P.-C. Tsai, S.-J. Wang - National Chung-Hsing University, Taiwan, ROC
4.6 : A Non Scan DFT Method using Functional Information of Operational Modules
H. Date, T. Hosokawa, M. Muraoka - Semiconductor Technology Academic Research Center, Japan

Banquet (Garden room, Hotel Fujita 1F)
18:30 - 20:30

Nov. 23, 2001

Session 5
9:00 - 10:15 (75-min)
Chair : Z. Li

5.1 : High-Level Analysis for Effective Test
J. A. Abraham - The University of Texas at Austin, U.S.A.
5.2 : Test Requirement Analysis for Low Cost Hierarchical Test Path Construction
Y. Makris - Yale University, U.S.A.
A. Orailoglu - U. C. San Diego, U.S.A.
5.3 : A design for hierarchical testability for RTL data paths using extended data flow graphs
S. Nagai, S. Ohtake, H. Fujiwara - Nara Institute of Science and Technology, Japan

Session 6
10:40 - 11:30 (60-min)
Chair : H. Li
6.1 : Low Power Test Compatibility Classes: Exploiting regularity for simultaneous reduction in test application time and power dissipation
N. Nicolici - McMaster University, Canada
B. M. Al-Hashimi - University of Southampton, U.K.
6.2 : Test Power Reduction for Full Scan Sequential Circuits by Test Vector Modification
S. Kajihara, K. Ishida, K. Miyase - Kyushu Institute of Technology, Japan

Lunch
11:30 - 13:00

Session 7
13:00 - 14:40 (100-min)
Chair : S. Xu

7.1 : Path Delay Test Generation for Standard Scan Designs Using State Tuples
Y. Shao, S. M. Reddy - University of Iowa, U.S.A.
I. Pomeranz - Purdue University, U.S.A.
7.2 : Compact TPG Design for a Deterministic BIST Scheme
T. Hayashi, T. Suzuki, T. Shinogi, H. Kita, H. Takase - Mie University, Japan
7.3 : Efficient RT-level Test Generation Techniques based on Refinement of Finite-state Machines
H. Li, Y. Min - Chinese Academy of Sciences, China
7.4 : A Compacted Test Plan Table Generation Method for RTL Data Path Circuits
T. Hosokawa, H. Date, M. Muraoka - Semiconductor Technology Academic Research Center, Japan

Tour
14:40 -
Todaiji Temple tour (the Great Buddha etc.)

Regular Session

Nov. 22

Opening

9:00 - 9:15

Invited talk

9:15 - 10:00

VCore Based Design Technology for the Next Generation SOC

M. Muraoka - Semiconductor Technology Academic Research Center, Japan

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10:20 - 12:00

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S. Mourad - Santa Clara University, U.S.A.

Lunch

Steering Committee Meeting (members only)

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2.1 : Design for Consecutive Testability of Systems-on-a-Chip with Built-In Self Testable Cores

T. Yoneda, H. Fujiwara - Nara Institute of Science and Technology, Japan

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K. S. Kim - Intel Corporation, U.S.A.

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R. Velazco, F. Faure - TIMA Laboratory, France

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P.-C. Tsai, S.-J. Wang - National Chung-Hsing University, Taiwan, ROC

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H. Date, T. Hosokawa, M. Muraoka - Semiconductor Technology Academic Research Center, Japan

Banquet

18:30 - 20:30

Nov. 23

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9:00 - 10:15

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T. Hosokawa, H. Date, M. Muraoka - Semiconductor Technology Academic Research Center, Japan

Tour

15:00 -

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return to the top page

REGISTRATION

 Advance registration instructions and Registration Form (PDF)  (text)

Click right buttm on your mouse to save this file

ADVANCE REGISTRATION INSTRUCTIONS

Advance registration due: October 20, 2001

To register, mail or fax your complete registration form with payment to:

Hiroshi Yokoyama, WRTLT'01 Finance Chair

Dept. of Computer Sci. and Eng. , Akita University

1-1 Tegata Gakuen-cho, Akita-shi, Akita 010-8502, JAPAN

Phone: +81-18-889-2776

Fax: +81-18-837-0408

E-mail: yokoyama@ie.akita-u.ac.jp

No registration form will be accepted after November 9, 2001 (postmarked cut-off).

After November 9, 2001, there will be on-site registration only.

Registration Fee:

Workshop registration fee includes admission to all technical sessions, coffee breaks, reception, banquet and a copy of the workshop digest of papers. The student fee does not include banquet. The banquet ticket may be purchased separately by accompanying persons and students for 6,000 yen per person.

Before Oct 20, 2001:

IEEE/CS Member	Non-Member	Student
22,000 yen	30,000 yen	8,000 yen

After Oct 20, 2001:

IEEE/CS Member	Non-Member	Student
27,000 yen	36,000 yen	10,000 yen

Payment:

- Payment by bank transfer: (recommend)

  The account name must be written as:

  WRTLT FINANCE YOKOYAMA HIROSHI

  Account No. 668455

  Tegata Branch (Branch # 133), Akita Bank (Bank # 0119), Akita, Japan

- Payment by bank draft:

  Make sure to indicate WRTLT FINANCE YOKOYAMA HIROSHI and your name on it.

- Payment by credit card: Unavailable.

Refund Policy:

No refunds will be made unless written request for cancellation is received prior October 20, 2001.

For Japanese:

日本国内からの送金は銀行振込みでお願いいたします。上記口座は，日本語では以下のようになります。

WRTLT FINANCE 横山洋之，または WRTLT FINANCE ヨコヤマヒロシ
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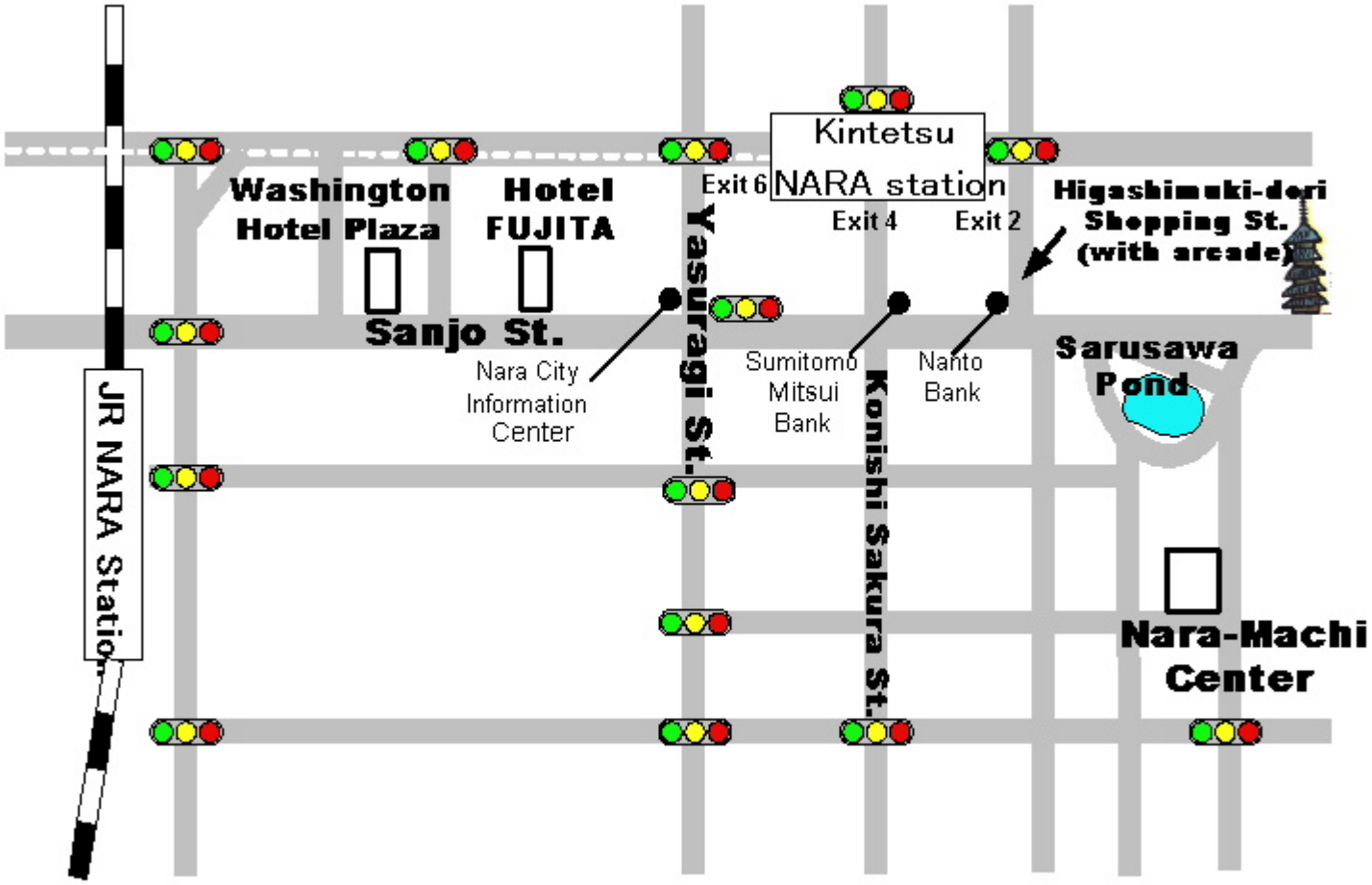
Kintetsu
NARA station
Exit 6
Exit 4
Exit 2
Washington
Hotel Plaza
Hotel
FUJITA
Sanjo St.
Yasuragi St.
Konishi Sakura St.
JR NARA Station
Nara City
Information
Center
Sumitomo
Mitsui
Bank
Nanto
Bank
Higashimuki-dori
Shopping St.
(with arcade)
Sarusawa
Pond
Nara-Machi
Center

Hotel Reservation Sheet

Please complete this form and send to:

Hotel Fujita Nara (47-1 Shimosanjo-cho, Nara-city, Nara 630-8236 Japan)
Facsimile: +81-742-22-0255
Telephone: +81-742-23-8111

The hotel will let you know whether acceptable or not after it would receive this sheet.

Please send it by ***2001/10/31***.

PARTICIPATION:

WRTLT'01 (Workshop on RTL ATPG & DFT) (2000/11/22-23)

Name _____

Address _____

City _____ **Country** _____

Telephone _____ **Facsimile** _____

I shall be accompanied by: **Name** _____

Check-in Date _____ **Check-out Date** _____ **Stay nights** _____

Room type: Please mark below which room you want to stay

For one person

_____ **Single room** 8,500 yen (per night)

_____ **Twin room** for single use 13,000 yen (per night)

For two persons

_____ **Twin room** 8,000 yen (per night and per one person)

Room charges include breakfast and service fare, but exclude tax.

Please mark below which room you want to stay

_____ **Non Smoking room** _____ **Smoking room**

Signature _____ **Date** _____

Hotel Reservation Sheet

Please complete this form and send to:

NARA WASHINGTON HOTEL PLAZA (31-1 Shimosanjo-cho, Nara-city, Nara 630-8236 Japan)
Facsimile: +81-742-27-0484
Telephone: +81-742-27-0410

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Room type: Please mark below which room you want to stay

For one person

_____ **Single room** 8,500 yen (per night)

Room charges include breakfast and service fare, but exclude tax.

Please mark below which room you want to stay

_____ **Non Smoking room** _____ **Smoking room**

Signature _____ **Date** _____

CALL FOR PAPERS WRTLT'01

Workshop on RTL ATPG & DFT

November 22-23, 2001, Naramachi-Center, Nara, Japan

Sponsored by

IEEE Computer Society Test Technology Technical Council

In Cooperation with

Technical Group on Fault Tolerant Systems, IEICE

General Chair

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Program Committee

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Topics of interest include (but not limited to):

- Functional fault modeling
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- Relationship between RT-level and gate-level testing

IMPORTANT DATES

Submission : July 31, 2001
Acceptance : August 31, 2001
Final version : to be announced

- Submissions must be made as Postscript or PDF attachments to e-mail sent to **wrtlt@info.eei.metro-u.ac.jp**
- Submissions must be a complete paper of 10 pages maximum, or an extended summary from four to six pages.
- The title page must include abstract, keywords, full mailing address, telephone and Fax number and e-mail address.
- An author of every accepted paper must present at the workshop

For up-to-date information refer to the WRTLT'01 website

http://wrtlt.ie.akita-u.ac.jp/wrtlt/

or contact the workshop chairs.

Nara is an ancient capital of Japan. In the end of November, you can enjoy not only a beautiful combination of red and yellow autumnal leaves but also historical shrines and temples. For more on tourism, a couple of links will be found at the above site.

WRTLT Steering Committee

Chair: Yinghua Min, Academia Sinica, China

Members:

Hideo Fujiwara, NAIST, Japan
Kazuhiko Iwasaki, Tokyo Metropolitan University, Japan
Xiaowei Li, Peking University, China
Kewal K. Saluja, University of Wisconsin, USA
Hideo Tamamoto, Akita University, Japan
J. Paulo Teixeira, IST/INESC, Portugal
Dafang Zhang, Hunan University, China

C A L L F O R P A P E R S

WRTLT'01

Workshop on RTL ATPG & DFT

Nara, Japan

November 22-23, 2001

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lxw@pku.edu.cn
Financial Chair:
Hiroshi Yokoyama, Akita University, Japan
yokoyama@ie.akita-u.ac.jp
Local Arrangements Chair:
Michiko Inoue, NAIST, Japan
kounoe@is.naist-nara.ac.jp

Program Committee Members:
Satoshi Fukumoto, Tokyo Metropolitan University, Japan
Sandeep K. Gupta, University of Southern California, USA
Kazumi Hatayama, Hitachi, Ltd., Japan
Terumine Hayashi, Mie University, Japan
Toshinori Hosokawa, STARC, Japan
Weikang Huang, Fudan University, China
Tomoo Inoue, Hiroshima City University, Japan
Zhongcheng Li, ICT, Chinese Academy of Sciences, China
Toshimitsu Masuzawa, Osaka University, Japan
Kewal K. Saluja, University of Wisconsin-Madison, USA
Yihe Sun, Tsinghua University, China
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Xiaoqing Wen, Syntest Tech., USA
Cheng-Wen Wu, Tsing Hua University, Taiwan
Shiyi Xu, Shanghai University, China
Hee Yong Youn, SungKyunKwan University, Korea
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Kewal K. Saluja, University of Wisconsin, USA
Hideo Tamamoto, Akita University, Japan
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WRTLT'01 The Second Workshop on RTL ATPG & DFT

November 22-23, 2001, Nara, Japan

(Naramachi-center, 38 Higashiterabayashi-cho, Nara-shi, Nara 630-8362, Japan)

Sponsored by *IEEE Computer Society Test Technology Technical Council*
In cooperation with *Technical Group on Fault Tolerant Systems, IEICE*

Website for WRTLT'02 : http://www.ip.elec.mie-u.ac.jp/~wrtlt02/

SCOPE

The Workshop on RTL ATPG & DFT (WRTLT) provides an international forum for interchanging ideas and implementation experiences on register transfer (RT) level automatic test pattern generation (ATPG) and design for testability (DFT). For systems on chip (SOC) devices, it has become a real hot topic to improve VLSI testability using high-level descriptions. Now in its 2nd year, just after the ATS'01, papers are solicited on all aspects of RT-level testing techniques. Photocopies of accepted papers will be handed out at the workshop site. We hope and expect the workshop will provide all participants with new ideas and food for thought through informal interactions and discussions.

Topics of interest include(but not limited to)

- Functional fault modeling
- RT-level ATPG
- RT-level DFT
- RT-level BIST
- Relationship between RTL and gate level testing

IMPORTANT DATES

- Submission: ~~July 31, 2001 => twelve noon, August 10, Japan Standard Time.~~
- Acceptacnce: ~~August 31, 2001~~
- Final version: ~~to be announced~~
- Registration: ~~Advance registraton due: October 20, 2001~~
  => **On-site registration**
- **Reception:** **November 21, 2001. 19:00-21:00.**
  At a restaurant, "Kissa Naramachi", 1st Floor, Naramachi Center.
  (Snack and drink will be served. Please join.)
- **Workshop:** **November 22-23, 2001**

For up-to-date information refer to this WRTLT'01 web site or contact the workshop chairs.

Final Program (Updated 11/15 2001)

WRTLT'01 Final Program (11/15 2001)

WRTLT'01 Advance Program (Updated 10/06 2001)

Registration (Updated 9/19 2001)

Advance Registration Instruciotns and **Registration Form**

Advance registration due: October 20, 2001

Access & Accommodations (Updated 11/01 2001, access to Nara)

Access

You can find an access to Nara here. If you come to Nara from Kyoto after ATS'01, we recommend to use a Kintetsu line other than a JR line. KINTETSU Kyoto station is adjacent to JR Kyoto station, and both are close to Righa Royal Hotel KYOTO (the place of ATS'01). Here is a MAP around Nara-Machi center and stations. KINTETSU Nara station is an underground station. If you go to the hotels, use the EXIT 4 and go up to the ground. If you go to Nara-Machi center, use the EXIT 2.

Accommodations

We keep some rooms for WRTLT'01 participants in Hotel Fujita NARA (English page) and NARA Washington Hotel Plaza (Japanese page). We also hold a banquet at Hotel Fujita NARA. Please use the following Hotel Reservation Form. For guaranteed reservation send the completed form by Oct. 31, 2001 to the HOTEL.

Hotel Fujita NARA (PDF, Word) (Updated 10/18 2001, Fax number was incorrect)
Nara Washington Hotel Plaza (PDF, Word)(Updated 9/18 2001)

Call for Papers

PDF version TEXT version

Organization

General Chair

Hideo Tamamoto (Akita University, Japan) tamamoto@ie.akita-u.ac.jp

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Michiko Inoue (NAIST, Japan) kounoe@is.aist-nara.ac.jp

Program Commitee

S. Fukumoto, Japan	T. Inoue, Japan	X. Wen, USA
S. Gupta, USA	Z. Li, China	C-W. Wu, Taiwan
K. Hatayama, Japan	T. Masuzawa, Japan	S. Xu, China
T. Hayashi, Japan	K. Saluja, USA	H. Youn, Korea
T. Hosokawa, Japan	Y. Sun, China	D. Zhang, China
W. Huang, China	J. P. Teixeira, Portugal	

WRTLT Steering Committee

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Yinghua Min (Academia Sinica, China)

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Kazuhiko Iwasaki (Tokyo Metropolitan University, Japan)
Xiaowei Li (Peking University, China)
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Hideo Tamamoto (Akita University, Japan)
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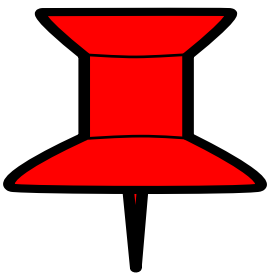
Dafang Zhang (Hunan University, China)
Alex Orailoglu (University of California, USA)

Links

- **Nara City Tourism Section's Home Page**
- **Nara Prefecture**
- **Nara City**
- **Naramachi-center (Japanese)**
- **ATS'01 Web site**

埋め込まれた保護文書

ファイル*http://wrtlt.ie.akita-u.ac.jp/wrtlt/registration/WRTLT01_registration_form.pdf*は、この文書に埋め込まれた保護文書です。表示するには、押しピンアイコンをダブルクリックしてください。



Registration Form

WRTLT'01, Workshop on RTL ATPG & DFT, Nara, Japan

November 22-23, 2001

Please complete by typing or printing in block letters.

Title: Prof. Dr. Mr. Ms.

Family name: _____

First name: _____

Middle Name: _____

Affiliation / Company:

_____

_____

Mailing Address: (office / Home)

_____

Phone: _____

Fax: _____

E-mail: _____

IEEE/CS Member No.: _____

Accompanying person, if any:

_____

Registration Fee(Check one of them):

Before Oct 20, 2001:

IEEE/CS Member	Non-Member	Student
22,000 yen	30,000yen	8,000 yen

After Oct 20, 2001:

IEEE/CS Member	Non-Member	Student
27,000 yen	36,000 yen	10,000 yen

Payment (Check one of them):

I will remit/have remitted the fee on _____(date)

under the name of _____(name of remitter)

to the account of:

WRTLT FINANCE YOKOYAMA HIROSHI

Account No. 668455

Tegata Branch (Branch # 133)

Akita Bank (Bank # 0119), Akita, Japan

I enclose herewith a bank draft for the fees payable to the

WRTLT FINANCE YOKOYAMA HIROSHI

Payment by credit card is not available.

Advance Registration Deadline: October 20, 2001

To register, mail or fax this form (or a copy of this form)

with payment to:

Hiroshi Yokoyama, WRTLT'01 Finance Chair

Dept. of Computer Sci. and Eng. , Akita University

1-1 Tegata Gakuen-cho, Akita-shi, Akita 010-8502, JAPAN

Phone: +81-18-889-2776

Fax: +81-18-837-0408

E-mail: yokoyam@ie.akita-u.ac.jp

No registration form will be accepted

after November 9, 2001 (postmarked cut-off).

After November 9, 2001, there will be on-site registration only.