The Tenth IEEE Workshop on RTL and High Level Testing

WRTLT '09

November 27-28,
The Chinese University of Hong Kong,
Hong Kong SAR, China

WRTLT- November 27-28, 2009

The purpose of this workshop is to bring researchers and practitioners on LSI testing from all over the world together to exchange ideas and experiences on register transfer level (RTL) and high level testing.

New: Hyatt hotel reservation

New: advance program and registration details.

Program Highlights:

keynote speech by **Jocob Abraham**, UT-Austin Univ.

Invited talk I by **Nicola Nicolici**, McMaster Univ.

Invited talk II by **Xinli Gu**, Cisco Systems, Inc.

Panel: Test / Diagnosis at Multi-Core / Multi-Die Era

Key Dates	
Submission:	**extended to Aug. 15th**
Acceptance:	**Sep.11th**
Camera Ready:	**Oct.10th**
Early Registration:	**Oct.25th**
Workshop:	**Nov.27th-28th**

WRTLT Topics

Areas of interest include but are not limited to:

- Functional fault modeling
- Microprocessor testing
- Relationship between RTL and gate level testing
- High level test bench generation
- High level approaches for testing
- RTL ATPG
- RTL BIST
- Design verification
- SoC testing
- RTL DFT

Sponsors

IEEE IEEE COMPUTER SOCIETY tttc EiC ICT

WRTLT- November 27-28, 2009

The purpose of this workshop is to bring researchers and practitioners on LSI testing from all over the world together to exchange ideas and experiences on register transfer level (RTL) and high level testing.

New: Hyatt hotel reservation

New: advance program and registration details.

Program Highlights:

keynote speech by **Jocob Abraham**, UT-Austin Univ.

Invited talk I by **Nicola Nicolici**, McMaster Univ.

Invited talk II by **Xinli Gu**, Cisco Systems, Inc.

Panel: Test / Diagnosis at Multi-Core / Multi-Die Era

Key Dates	
Submission:	**extended to Aug. 15th**
Acceptance:	**Sep.11th**
Camera Ready:	**Oct.10th**
Early Registration:	**Oct.25th**
Workshop:	**Nov.27th-28th**

WRTLT Topics

Areas of interest include but are not limited to:

- Functional fault modeling
- Microprocessor testing
- Relationship between RTL and gate level testing
- High level test bench generation
- High level approaches for testing
- RTL ATPG
- RTL BIST
- Design verification
- SoC testing
- RTL DFT

Sponsors

version 2

WRTLT'09 Advance Program

November 27--28, 2009

November 27 (Friday)

Registration **8:00 -- 8:40**

Opening session **8:40 -- 9:00**

Keynote speech **9:00 -- 10:00**

System-Level Verification and Test: From Microprocessors to SoCs and Multicore Chips

Jacob Abraham (UT Austin -- USA)

Coffee break **10:00 -- 10:30**

Session 1 **RTL and High-Level Testing** **10:30 -- 11:50**

Chair: Tomoo Inoue *(Hiroshima City University -- Japan)*

1.1 A DFT Method for Functional Scan at RTL

Marie Engelene, J. Obien and Hideo Fujiwara (Nara Institute of Science and Technology -- Japan)

1.2 Observation-Point Selection at Register-Transfer Level to Increase Defect Coverage for Functional Test Sequences

Hongxia Fang 1, Krishnendu Chakrabarty 1 and Hideo Fujiwara 2 (1 Duke University – USA, 2 Nara Institute of Science and Technology -- Japan)

1.3 A Study of Software-Level Delay Fault Simulation for JPEG Decoder Application on CMP

Shun-Yen Lu, Tso-Hua Chien and Jing-Jia Liou (National Tsing Hua University -- Taiwan)

1.4 Path-Based Resource Binding to Reduce Delay Fault Test Cost

Michiko Inoue, Satoshi Ohtake, Yu-ichi Uemoto, and Hideo Fujiwara (Nara Institute of Science and Technology -- Japan)

Lunch & Poster **12:00 -- 13:30**

Invited talk **13:30 -- 14:15**

A research perspective on post-silicon validation and debug

Nicola Nicolici (McMaster Univ. -- Canada)

Session 2 **Low-Power Testing** **14:20 -- 15:20**

Chair: Xiaoqing Wen *(Kyushu Institute of Technology -- Japan)*

2.1 Low Capture Power Adjacent Fill (LCPAF) in Test Data Compression Environment

Jia Li 1, Qiang Xu 2 and Dong Xiang 1 (1 Tsinghua University – China, 2 The Chinese University of Hong Kong – Hong Kong)

2.2 Scan Cells Reordering to Minimize Peak Power during Scan Testing of SoC

Jaynarayan T Tudu 1, Erik Larsson 2, Virendra Singh 1, and Hideo Fujiwara 3 (1. Indian Institute of Science –India, 2. Linkoping University – Sweden, 3. Nara Institute of Science and Technology -- Japan)

2.3 Efficient Modeling of IR-Drop Using Dynamic SDF for Test and Diagnosis

Ke Peng 1, Yu Huang 2, Wu-Tung Cheng 2, and Mohammad Tehranipoor 1 (1 University of Connecticut -- USA, 2 Mentor Graphics -- USA)

Coffee break 15:20 -- 15:40

Session 3 Fault Simulation and Test Generation 15:40 -- 17:00

Chair: Jing-Jia Liou *(National Tsing Hua University -- Taiwan)*

3.1 A Fast and Memory-Efficient Fault Simulation Using GPU

Dawen Xu, Yinhe Han, Huawei Li, and Xiaowei Li (Chinese Academy of Sciences -- China)

3.2 Test Generation for Open Faults Considering the Effects of Adjacent Lines

Ryota Kuribayashi, Hiroyuki Yotsuyanagi, and Masaki Hashizume (The Univ. of Tokushima -- Japan)

3.3 Compact Test Generation for Complete Coverage of Path Delay Faults in a Standard Scanned Circuit

Dong Xiang and Zhen Chen (Tsinghua University – China)

3.4 X-Identification According to Required Distribution for Industrial Circuits

Isao Beppu, Kohei Miyase, Yuta Yamato, Xiaoqing Wen,and Seiji Kajihara (Kyushu Institute of Technology -- Japan)

Panel 17:00 -- 18:30

Test / Diagnosis at Multi-Core / Multi-Die Era

Organizer and Moderator: Yu Huang (Mentor Graphics -- USA)

Panelists: Kazumi Hatayama (STARC -- Japan)
Zebo Peng (Linkoping University -- Sweden)
Yasuo Sato (Kyushu Institute of Technology -- Japan)
James Chien-Mo Li (National Taiwan University -- Taiwan)
Ilia Polian (Albert Ludwigs University of Freiburg -- Germany)

Social Event 18:30 -- 22:30

November 28 (Saturday)

Invited talk 8:30 -- 9:15

Quality, Cost and Time-to-Market: We Need Them All

Xinli Gu (Cisco -- USA)

Session 4 Design for Testability 9:20 -- 11:00

Chair: Ilia Polian *(Albert Ludwigs Univ. of Freiburg -- Germany)*

4.1 Is the Full Scan Design Unshakeable?

Yinhua Min (Chinese Academy of Sciences -- China)

4.2 A Design of Concurrently Testable Response Analyzers in Built-in Self-Test

Yuki Fukazawa, Yuki Yoshikawa, Hideyuki Ichihara,and Tomoo Inoue (Hiroshima City University -- Japan)

4.3 A Low Cost Self-Hold Analog Test Wrapper Design for Mixed-Signal SOCs

Yang Jin, Hong Wang, and Shiyuan Yang (Tsinghua University – China)

4.4 Improving Transition Delay Fault Coverage with Partial Enhanced Scan Technique

Songwei Pei, Huawei Li, and Xiaowei Li (Chinese Academy of Sciences -- China)

4.5 Scan Slice Compression Technique Using Dynamical Updating Reference Slices

Jun Liu, Yinhe Han, and Xiaowei Li (Chinese Academy of Sciences -- China)

Coffee break 11:00 -- 11:20

Session 5 Diagnosis and Fault-Tolerance 11:20 -- 12:40

Chair**: Huawei Li** *(Chinese Academy of Sciences -- China)*

5.1 Diagnosis of Logic-chain Bridging Faults

#Wei-Chih Liu, Wei-Lin Tsai, Hsiu-Ting Lin,and James Chien-Mo Li (National Taiwan University -- Taiwan)

5.2 An Even-Odd DFD Technique for Scan Chain Diagnosis

Venkat Rajesh A 1, Erik Larsson 2,Virendra Singh 3, and MS Gaur 1 (1 Indian Institute of science – India, 2 Linkoping University – Sweden, 3 Malaviya National Instituet of Technology -- India)

5.3 Transition Fault Diagnosis Using At-speed Test Patterns

Shang-Feng Chao, Jheng-Yang Ciou, and James Chien-Mo Li (National Taiwan University -- Taiwan)

5.4 On Predicting the Maximum Circuit Aging

Song Jin, Yinhe Han, Huawei Li, and Xiaowei Li (Chinese Academy of Sciences -- China)

Poster

1 The Impact of Performance Asymmetry on Topology Reconfiguration in NoC-based Many-core Systems

Yue Yu 1, Lei Zhang 1, Jianbo Dong 1, Yinhe Han 1, and Shangpin Ren 2 (1 Chinese Academy of Sciences – China, 2 Illinois Institute of Technology -- USA)

2 A Thermal-aware Parallel Multicast Testing Method Based on Many-core Chips

Fang Fang 1, Wei Wang 1, Yinhe Han 2, and Xiaowei Li 2 (1 Hefei University of Technology – China, 2 Chinese Academy of Sciences – China)

3 A Particle Swarm Optimization-based BPNN Approach for Fault Diagnosis of Analog Electronic Circuits

Wenji Zhu and Yigang He (Hunan University -- China)

4 Microprocessor Modeling for Board Level Test Access Automation

Sergei Devadze 1, Artur Jutman 1, Anton Tsertov 2, and Raimund Ubar 2 (1 Testonica Lab Oü – Estonia, 2 Tallinn Univ. of Technology -- Estonia)

5 Hierarchical Formal Verification Method based on Transactions

Zhiqiu Kong, Jinian Bian, Yanni Zhao, and Shujun Deng (Tsinghua University – China)

6 Semi-Confliction Guided Problem Partitioning Algorithm in FPGA-based SAT Solver

Zhongda Yuan and Jinian Bian (Tsinghua University – China)

7 A Low Power Test Scheme Based on Segment Fixing Folding Counter

Tian Chen, Hua-guo Liang, Min-sheng Zhang, Wei Wang, and Mao-xiang Yi (Hefei University of Technology – China)

8 SORPECO: Localized SOR Analysis Method for Power/Ground Networks in ECO Placements

Zuying Luo 1, Guoxing Zhao 1, and Jinhe Zhou 2 (1 Beijing Normal University – China, 2. Beijing Information Science and Technology University -- China)

9 Modeling Test Flows of Automated Test Equipment Test Program Using Simple Graph

Hui Jia Tai 1, Chin Kuan Ho 1, Hze Horng Ong 2, Somnuk Phon-Amnuaisuk 1, Siew Beng Thum 2 (1 Multimedia University – Malaysia, 2 Intel Corporation, -- Malaysia)

10 A Model for Scan Insertion at the Register Transfer Level

Lilia Zaourar 1, Yann Kieffer 1, Chouki Aktouf 2, Vincent Juliard 2
(1 G-SCOP laboratory – France, 2 DeFacTo Technologies -- France)

Scope

The purpose of this workshop is to bring researchers and practitioners on LSI testing from all over the world together to exchange ideas and experiences on register transfer level (RTL) and high level testing. WRTLT'09, the tenth workshop, will be held in Hong Kong SAR, China. We expect this workshop to provide an ideal forum for frank discussion on this important topic for the future system-on-a-chip (SoC) devices.

Areas of interest include but are not limited to:

- Functional fault modeling
- Microprocessor testing
- Relationship between RTL and gate level testing
- High level test bench generation
- High level approaches for testing
- RTL ATPG
- RTL BIST
- Design verification
- SoC testing
- RTL DFT

Submissions

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (1,000 words) or a full paper and should include: title, full name and affiliation of all authors, 50 words abstract, keywords and the name of contact author. All submissions should be sent to the following address as Postscript or PDF attachment.

Paper submission by E-mail:wrtlt09@cse.cuhk.edu.hk

The submission will be considered evidence that upon acceptance the author(s) will prepare the final manuscript in time for inclusion in the digests and will present the paper at the Workshop.

Registration Fee

Memberships	Until Oct. 25	After Oct. 25
IEEE member	USD$250	USD$310
Non-member	USD$320	USD$390
IEEE student member	USD$150	USD$180
Student non-member	USD$180	USD$200

Please note that:

a. IEEE Member rates are only available to individuals who are IEEE members at the time of registration - visit www.ieee.org to join.

b. Advanced registration is till October 25. No Registration form will be accepted after Novermber 10. After this date, please register on-site.

c. Please contact the Finance Chair, Mr. Yubin Zhang, for registration issues.

Email: ybzhang@cse.cuhk.edu.hk

Tel: +852 31634265

Fax: +852 26035024

Registration Procedure

1. Pay the registration fee through one of the following payment methods.
2. Fill out the registration form, sign it, and send to Mr. Yubin Zhang by email ybzhang@cse.cuhk.edu.hk or fax +852 26035024, if you don't choose the online payment.

Payment Methods

All payments will be made in US Dollars (USD$). Registration fees can be remitted by credit card (Visa and MasterCard) or bank transfer. Cash payments will only be accepted on site. Other methods of payment will not be accepted.

1. On-line credit card payment. Please input your registration information first, and the online payment can then be accessed.
2. Charge the credit card on registration form. The finance officer of WRTLT 2009 will charge your credit card, provided on the registration form, with the respective amount.
3. Pay by bank transfer. Please send your bank transfer receipt by email or fax after you have transfered the fee to the following account:

   Bank Name: Hang Seng bank Ltd Head Office

   Bank Address: 83 Des Voeux Road Central Hong Kong

Bank Swift Code: HASE HKHH

Bank Code: 024

Bank Account Number: 222265514882

Bank Account Name: Yubin Zhang

Please kindly present the bank transfer receipt at the registration desk. Please note that any additional transfer or service charges imposed by the bank must be paid by the participant. Please DO NOT allow your bank to deduct it from the registration fee.

Location:

Ho Sin-Hang Engineering Building, Room 121
The Chinese University of Hong Kong
Shatin, N.T., Hong Kong

How to get to CUHK: check here.

Map of CUHK (Building H25)

Visiting HK:

Visa requirement: check here.

If you need an invitation letter, please contact Local Arrangement Chair, Mr. Feng Yuan, fyuan@cse.cuhk.edu.hk.

Hotels:

The following hotels are nearby The Chinese University of Hong Kong.

Hyatt Hotel (5-star, Reservation with special rate)

Royal Park Hotel (4-star)

Regal Riverside Hotel (3-star)

For the above two hotels, we cannot provide special rate lower than online agency, e.g.,

Expedia.

System-Level Verification and Test: From Microprocessors to SoCs and Multicore Chips

Jocob Abraham

Advances in semiconductor technology have enabled the integration of many digital cores alon g with mixed-signal and RF modules on a single chip. While Systems on a Chip (SoCs) offer many benefits in cost and performance, they pose significant challenges for verifying the corre ctness of the design and for testing manufactured chips for defects. Verification of the design h as to deal with enormous state spaces. Tests for defects in nanometer scale technologies have to detect small delay variations, as well as deal with embedded analog and RF modules.

This talk will describe techniques which employ abstractions based on static analysis of the d esign description, and which exploit the hierarchy in the design. The abstractions can be gener ated efficiently, and the approach scales well with increasing design sizes and multiple cores. Applications to verification of complex designs demonstrate that improvements of several orde rs of magnitude in time can be achieved compared with conventional approaches. A new direct ion in at-speed test, called "native mode self-test" automatically maps test sequences for fault s in embedded modules to processor instructions. The processor can then be used to test other modules, including mixed-signal cores for analog and RF specifications. On-chip sensors can b e used to facilitate test of RF modules; chip measurements show that the approach can predict the specifications of the mixed-signal modules with high accuracy.

Jacob A. Abraham is Professor of Electrical and Computer Engineering and Professor of Comp uter Sciences at the University of Texas at Austin. He is also the director of the Computer En gineering Research Center and holds a Cockrell Family Regents Chair in Engineering. He rec eived his Ph.D. in Electrical Engineering and Computer Science from Stanford University in 1 974. His research interests include VLSI design and test, formal verification, and fault-tolera nt computing. He has published extensively and has been included in a list of the most cited r esearchers in the world. He has supervised more than 70 Ph.D. dissertations, and is particula rly proud of the accomplishments of his students, many of whom occupy senior positions in ac ademia and industry. He has been elected Fellow of the IEEE as well as Fellow of the ACM, a nd is the recipient of the 2005 IEEE Emanuel R. Piore Award.

A Research Perspective on Post-Silicon Validation and Debug

Nicola Nicolici

Post-silicon validation and debug is concerned with identifying design errors that escape to silicon. While commonly employed in practice, it has received significantly less research attention when compared to its complementary problem of manufacturing test, which is focused on screening for fabrication defects. In this talk we outline some recent advances in the field and highlight several challenges, including what can be addressed at the register transfer level.

Nicola Nicolici is an Associate Professor of Electrical and Computer Engineering at McMaster University. He received the Dipl. Ing. degree in Computer Engineering from the Politehnica University of Timisoara, Romania (1997) and a Ph.D. in Electronics and Computer Science from the University of Southampton, U.K. (2000). He is the recepient of the Best Student Paper Award at the IEEE International Test Conference (ITC) in 2000 and the Best Paper Award at the IEEE/ACM Design Automation and Test in Europe (DATE) in 2004.

Quality, Cost and Time-to-Market: We Need Them All

Xinli Gu

Electronic industry is under tremendous pressure of quality, cost and TTM (Time-To-Market). As an electronic system company, it faces very critical design schedule, quality component manufacture, system function bring-up challenges and system production manufacture. Adding quality control risks cost and TTM, but it is required in order to be successful in the market. In this presentation, the experience and practice of quality control at a telecommunication system company is presented. Quality is a very important measurement due to the nature of the application in this business. On the other hand, cost is also very sensitive due to the volume of the products shipped. Early design and complete planning for quality/test is a key to help us achieve this.

Xinli Gu is a director of Advanced Technology Group, Cisco Systems, Inc. He leads a large globalized team (SJ USA, RTP USA, Bangalore India, Chennai India and Shanghai China) within Cisco responsible for company-wide product manufacturing test quality and in-field reliability. He has a PhD in computer science from Linkoping University, Linkoping, Sweden.

Test / Diagnosis at Multi-Core / Multi-Die Era

Organizer: Yu Huang, Mentor Graphics
Panelists:
Dr. Kazumi Hatayama; STARC, Japan
Prof. Zebo Peng; Linkoping University, Sweden
Prof. Yasuo Sato; Kyushu Institute of Technology, Japan
Prof. James Chien-Mo Li; National Taiwan University, Taiwan
Prof. Ilia Polian; Albert Ludwigs University of Freiburg, Germany

This panel is to discuss/debate on the following test and diagnosis issues at the multi-core/multi-die era among the panelists and the audience.

(1) What would be the future trend of the design? SoC or SIP or both (different techniques will dominate different applications)?

(2) What are the advantages / disadvantages compare SoC vs. SIP?

(3) If you believe SoC will dominate in future, what are the test / diagnosis problems that have not been completely solved in multi-core designs? What solutions you believe are in the right direction?

(4) If you believe SIP (including 3-D techniques) will dominate in future, what are the test / diagnosis problems that have not been completely solved in multi-die design? What solutions you believe are in the right direction?

(5) Anything you feel is important and want to share about this topic?

Online Registration System

Please fill in your registration information.
(Items with * mark are mandatory.)

Personal Information

*Title	○ Prof. ○ Dr. ○ Mr. ○ Mrs. ○ Ms.
*Name	*Last Name (Surname) *First Name Middle Name
*Credit Card Holder Name	
*E-mail Address	
*E-mail Address Confirmation	
IEEE Member No	
Affiliation/Company	
Mailing Address	
Paper Title	

Go to Payment Page