Technical Program

Opening Session: Invited Talks

Invited Talk:

Session 1: RTL DFT

Chair:

S1-1 SREEP-2: SR-Equivalent Generator for Secure and Testable Scan Design
Katsuya Fujiwara, Hideo Fujiwara and Hideo Tamamoto

S1-2 Experimental Evaluation of Hybrid RTL Scan Design
Seiji Hirota, Ke Wang, Yuki Yoshikawa, Hideyuki Ichihara and Tomoo Inoue

S1-3 Testable and Built-In Self-Test Techniques for Motion Estimation Computing Arrays
Shyue-Kung Lu

S1-4 A Simulation-Based Feature Selection Approach for Test Point Selection in HDL Models
Nastaran Nemati, Seyyed Ehsan Mahmoudi, Amirhossein Simjour and Zeinalabedin Navabi

S1-5 Low-Power Wrapper Design for IP Cores Based on IEEE 1500 Standard
Yang Yu

Session 2: Design verification

Chair:

S2-1 Checking Pipelined Distributed Global Properties for Post-silicon Debug
Erik Larsson, Bart Vermeulen and Kees Goossens

S2-2 Transaction Level Formal Verification using Timed Automata
Amirali Ghofrani, Fatemeh Javaheri, Hamid Noori and Zainalabedin Navabi

S2-3 Study on Insertion Point and Area of Observation Circuit for On-Chip Debug Technique
Masayuki Arai, Yoshihiro Tabata and Kazuhiko Iwasaki

S2-4 VPLib: A Hybrid Method to Verify Microprocessor Prototypes on FPGA
Jingfen Lu, Lingkan Gong and Peng Ma

S2-5 Test Scheduling of Modular System-on-Chip under Capture Power Constraint
Jaynarayan Tudu, Erik Larsson, Virendra Singh

Session 3: SoC testing

Chair:

S3-1 Fast Detection and Analysis Schemes for System-in-Package in the Presence of RAM
Chia-Yi Lin, Yu-Wei Chen, Wang-Jin Chen and Hung-Ming Chen

S3-2 An Approach to Test Scheduling for Asynchronous On-Chip Interconnects Using Integer Programming
Tsuyoshi Iwagaki, Eiri Takeda and Mineo Kaneko

S3-3 Network-on-Chip Concurrent Error Recovery Using Functional Switch Faults
Naghmeh Karimi, Somayeh Sadeghi Kohan and Zainalabedin Navabi

S3-4 Test Wrapper Design for 3D System-on-Chip Using Optimized Number of TSVs
Surajit Kumar Roy, Saurav Ghosh, Hafizur Rahaman and Chandan Giri

Session 4: High level approach for testing

Chair:

S4-1 A Practical and Efficient Method to Test for Bridging Defects
Cynthia Hao and Colin.D Renfrew

S4-2 An Optimal HDL-based Approach for Mixed-level Hierarchical Fault Simulation
Nastaran Nemati, Arezoo Kamran, MohammadHossein Sargolzaie, MohammadHashem Haghbayan and Zainalabedin Navabi

S4-3 Multi-Level Test Package, A Package for C/C++ Gate Level Fault Simulation of System Level Design
Somayeh Sadeghi Kohan, Fatemh Javaheri, Sina Mahmoodi and Zainalabedin Navabi

S4-4 An Approach for Verification Assertions Reuse in RTL Test Pattern Generation
Maksim Jenihhin, Jaan Raik, Hideo Fujiwara, Raimund Ubar and Taavi Viilukas

S4-5 Test Vector Reduction by Reordering Flip-flops for Scan Architecture with Delay Fault Testability
Kiyonori Matsumoto, Kazuteru Namba and Hideo Ito

Session 5: Functional fault modeling, RTL ATPG & Relationship between RTL and gate level testing

Chair:

S5-1 A New Class of Acyclically Testable Sequential Circuits with Multiplexers
Nobuya Oka, Yuki Yoshikawa, Hideyuki Ichihara and Tomoo Inoue

S5-2 X-Identification of Transition Delay Fault Tests for Launch-off Shift Scheme
Kohei Miyase, Fangmei Wu, Luigi Dilillo, Alberto Bosio, Patrick Girard, Xiaoqing Wen and Seiji Kajihara

S5-3 A Comprehensive Functional Time Expansion Model Generation Method for Datapaths

Using Controllers
Toshinori Hosokawa, Teppei Hayakawa and Masayoshi Yoshimura

S5-4 Functional Fault Model for Micro Operation Faults of High Correlation with Stuck-At Faults
Chia Yee Ooi and Hideo Fujiwara

Session 6: Other

Chair:

S6-1 A Scalable Test Access Mechanism for Godson-T Multi-core Processor
Luning Kong, Yu Hu and Xiaowei Li

S6-2 Low-Power DLL-based On-Product Clock Generation for 3D Integrated Circuit Testing
Michael Buttrick and Sandip Kundu

S6-3 Clock Signal Modulation for IC Electromagnetic Compatibility
Felipe Lavratti, Leticia Maria Bolzani Pöhls, Jorge Semião, Fabian Vargas, Juan Rodriguez-Andina, Isabel Teixeira and João Paulo Teixeira

S6-4 Design for Efficient Speed-Binning and Circuit Failure Prediction and Detection
Songwei Pei, Huawei Li and Xiaowei Li