IEEE Eleventh Workshop on RTL and High Level Testing (WRTLT'10)

Shanghai SHERATON Hotel, Shanghai, P. R. China

December 5-6, 2010

Sponsored by

IEEE Computer Society Test Technology Technical Council

In Cooperation with

Shanghai Normal University

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National Natural Science Foundation of China(NSFC)

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Committee of Fault-tolerant Computing (CFTC)

WRTLT' 2010 - December 5-6, 2010

The purpose of this workshop is to bring researchers and practitioners on LSI testing from all over the world together to exchange ideas and experiences on register transfer level (RTL) and high level testing.

The eleventh workshop on RTL and high level testing (WRTLT'10) will be hold in conjunction with the 19th Asian Test Symposium (ATS'10) in Shanghai, China. We hope and expect this workshop provides an ideal forum for frank discussion on this important topic for the future system-on-a-chip (SoC) devices.

Important Dates

Submission deadline: July 27, 2010
Notification of acceptance: August 31, 2010
Camera-ready copy: September 20, 2010

Topics

Areas of interest includes but not limited to:

- Functional fault modeling
- RTL ATPG
- RTL DFT
- RTL BIST
- Relationship between RTL and gate level testing
- Design verification
- High level test bench generation
- SoC testing
- High level approach for testing
- Microprocessor testing

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Paper Submissions

Authors are invited to submit paper proposals for presentation at the workshop. The proposal
may be an extended summary (1,000 words) or a full paper and should includes: title, full name
and affiliation of all authors, 100 words abstract and 5 keywords. The full mailing address, phone, fax and email address of the corresponding author should be specified. All submissions must be made electronically in PDF format. Please visit our web site (http://wrtlt10.shnu.edu.cn)
for full submission instructions and updated information on the workshop.
Papers will be reviewed internationally and selected based on their originality, significance, relevance, and clarity of presentation. All accepted papers will be offered the possibility to be published in Journal of Shanghai Normal University.

The submissions will be considered evidence that upon acceptance the author(s) will prepare the
final manuscript on time for inclusion in the digests and will present the paper at the workshop.

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Keynote Speech

Low-Power Testing for Low-Power Devices

PRESENTER

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Speaker Biography

Xiaoqing Wen r

eceived the B.E. degree in computer science and technology from Tsinghua University, Beijing, China in 1986, the M.E. degree in information engineering from Hiroshima University, Hiroshima, Japan in 1990, and the Ph.D. degree in applied physics from Osaka University, Osaka, Japan in 1993. From 1993 to 1997, he was an Assistant Professor at Akita University, Akita, Japan. He was a Visiting Researcher at University of Wisconsin – Madison, USA, from October 1995 to March 1996. He joined SynTest Technologies, Inc., Sunnyvale, USA, in 1998 and served as its Chief Technology Officer until 2003. In 2004, he joined Kyushu Institute of Technology, Iizuka, Japan, where he is currently a Professor. He served as the Chair of Department of Creative Informatics in 2008 and 2009.

Dr. Wen's research interests include test, testable design, and diagnosis of VLSI circuits. He currently holds 23 U.S. Patents and 5 Japan Patents in built-in self-test, test compression, and low-power test generation. He received the 2008 Society Best Paper Award from Institute of Electronics, Information and Communication Engineers – Information Systems Socisety for his pioneering work in low-capture power test generation. He co-authored and co-edited two books: VLSI Test Principles and Architectures: Design for Testability (San Francisco: Morgan Kaufmann, 2006) and Power-Aware Testing and Test Strategies for Low Power Devices (New York: Springer, 2009). He was the Program Committee Co-Chair of the Sixteenth IEEE Asian Test Symposium and the Eighth IEEE Workshop on RTL and High Level Testing. He is currently on numerous program committees, including IEEE/ACM Design Automation Conference (DAC), IEEE International Test Conference (ITC), Design, Automation, and Test in Europe (DATE), IEEE European Test Symposium (ETS), and IEEE Asian Test Symposium (ATS). He is the Associate Editor for the Information Processing Society Transactions on System LSI Design Methodology, Journal of Computer Science and Technology, and Journal of VLSI and Electronic System Design.

Dr. Wen is a Senior Member of IEEE, a Member of the IEICE, the IPSJ, and the REAJ.

Abstract

Low-power devices are indispensable for modern electronic applications, and numerous hardware/software techniques have been developed for drastically reducing functional power dissipation. However, the testing of such low-power devices has increasingly become a severe challenge, especially in at-speed scan testing where a transition is launched at the output of a flip-flop and the corresponding circuit response is captured by a flip-flop with a functional clock pulse. The reason is that most or all of the functional constraints with respect to circuit operations and clocking are ignored in at-speed scan testing, which may result in test power that is several times higher than functional power.

Excessive test power may cause die/package damage due to excessive heat as well as undue yield loss due to excessive power supply noise, as illustrated in Figure 1. As a result, it has become imperative to apply low-power testing to low-power devices. That is, low-power devices cannot be successfully realized without effective and efficient low-power test solutions.

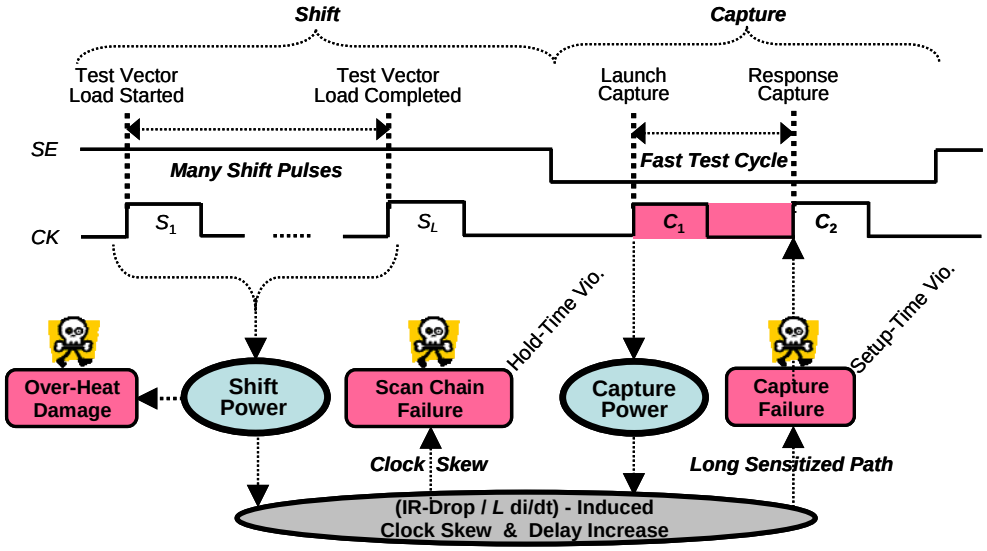

Figure 1. Impact of Test Power in LOC-Based At-Speed Scan Testing

This presentation first describes the basics of power dissipation in CMOS circuits. It goes on to highlight the difference between power dissipation in function mode and power dissipation in test mode, and lists the reasons why test power may become several times higher than functional power for low-power device. This presentation then describes the widely used clocking scheme for at-speed scan testing, namely launch-on-capture (LOC), and shows the different characteristics of shift power and capture power in LOC-based at-speed scan testing. Based on that, a general low-power testing strategy is outlined, featuring the use of design-for-test (DFT) for reducing shift power and the use of test data manipulation for reducing capture power. This presentation then provides a comprehensive review of the state-of-the-art techniques for reducing shift and capture power. Finally, future trends in the research and development for more advanced and sophisticated low-power testing solutions for low-power devices are discussed.

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Panel Session

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ADVANCE PROGRAM

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(WRTLT'10)

No.	December 4, 2010 (Wednesday)		
1	**Day 0 Reg.**	14:00 – 20:30	Registration (Front desk)
2		18:00 – 20:30	Welcome Reception
3	**December 5, 2010 (Sunday)**		
4	**Day 1 Reg.**	9:00 – 9:40	Opening Session **1** (Room A)
5		9:40 – 10:00	Coffee Break 1
6		10:00 – 11:15	Plenary Session **2** (Keynote Speech) (Room A)
7		11:15– 13:00	**Lunch Time 1**
8		13:00 – 15:00	Session 1 (Room A) 4 papers
9		15:00 – 15:20	Coffee Break 2
10		15:20 – 17:20	Session 2 (Room A) 4 papers
17		18:30 – 21:00	**Night Banquet**
11	**December 6, 2009 (Monday)**		
12	**Day2 Reg.**	8:00 – 10:00	Session 3 (Room A) 4 papers
13		10:00 – 10:20	Coffee Break 3
14		10:20 – 12:20	Session 4 (Room A) 4 papers
15		12:20 – 13:20	**Lunch Time 2**
12		13:20 – 15:20	Session 5 (Room A) 4 papers
13		15:20 – 15:40	Coffee Break 4
14		15:40 – 17:40	Session 6 (Room A) 4 papers

Technical Program

Opening Session: Invited Talks

Invited Talk:

Session 1: RTL DFT

Chair:

S1-1 SREEP-2: SR-Equivalent Generator for Secure and Testable Scan Design
Katsuya Fujiwara, Hideo Fujiwara and Hideo Tamamoto

S1-2 Experimental Evaluation of Hybrid RTL Scan Design
Seiji Hirota, Ke Wang, Yuki Yoshikawa, Hideyuki Ichihara and Tomoo Inoue

S1-3 Testable and Built-In Self-Test Techniques for Motion Estimation Computing Arrays
Shyue-Kung Lu

S1-4 A Simulation-Based Feature Selection Approach for Test Point Selection in HDL Models
Nastaran Nemati, Seyyed Ehsan Mahmoudi, Amirhossein Simjour and Zeinalabedin Navabi

S1-5 Low-Power Wrapper Design for IP Cores Based on IEEE 1500 Standard
Yang Yu

Session 2: Design verification

Chair:

S2-1 Checking Pipelined Distributed Global Properties for Post-silicon Debug
Erik Larsson, Bart Vermeulen and Kees Goossens

S2-2 Transaction Level Formal Verification using Timed Automata
Amirali Ghofrani, Fatemeh Javaheri, Hamid Noori and Zainalabedin Navabi

S2-3 Study on Insertion Point and Area of Observation Circuit for On-Chip Debug Technique
Masayuki Arai, Yoshihiro Tabata and Kazuhiko Iwasaki

S2-4 VPLib: A Hybrid Method to Verify Microprocessor Prototypes on FPGA
Jingfen Lu, Lingkan Gong and Peng Ma

S2-5 Test Scheduling of Modular System-on-Chip under Capture Power Constraint
Jaynarayan Tudu, Erik Larsson, Virendra Singh

Session 3: SoC testing

Chair:

S3-1 Fast Detection and Analysis Schemes for System-in-Package in the Presence of RAM
Chia-Yi Lin, Yu-Wei Chen, Wang-Jin Chen and Hung-Ming Chen

S3-2 An Approach to Test Scheduling for Asynchronous On-Chip Interconnects Using Integer Programming
Tsuyoshi Iwagaki, Eiri Takeda and Mineo Kaneko

S3-3 Network-on-Chip Concurrent Error Recovery Using Functional Switch Faults
Naghmeh Karimi, Somayeh Sadeghi Kohan and Zainalabedin Navabi

S3-4 Test Wrapper Design for 3D System-on-Chip Using Optimized Number of TSVs
Surajit Kumar Roy, Saurav Ghosh, Hafizur Rahaman and Chandan Giri

Session 4: High level approach for testing

Chair:

S4-1 A Practical and Efficient Method to Test for Bridging Defects
Cynthia Hao and Colin.D Renfrew

S4-2 An Optimal HDL-based Approach for Mixed-level Hierarchical Fault Simulation
Nastaran Nemati, Arezoo Kamran, MohammadHossein Sargolzaie, MohammadHashem Haghbayan and Zainalabedin Navabi

S4-3 Multi-Level Test Package, A Package for C/C++ Gate Level Fault Simulation of System Level Design
Somayeh Sadeghi Kohan, Fatemh Javaheri, Sina Mahmoodi and Zainalabedin Navabi

S4-4 An Approach for Verification Assertions Reuse in RTL Test Pattern Generation
Maksim Jenihhin, Jaan Raik, Hideo Fujiwara, Raimund Ubar and Taavi Viilukas

S4-5 Test Vector Reduction by Reordering Flip-flops for Scan Architecture with Delay Fault Testability
Kiyonori Matsumoto, Kazuteru Namba and Hideo Ito

Session 5: Functional fault modeling, RTL ATPG & Relationship between RTL and gate level testing

Chair:

S5-1 A New Class of Acyclically Testable Sequential Circuits with Multiplexers
Nobuya Oka, Yuki Yoshikawa, Hideyuki Ichihara and Tomoo Inoue

S5-2 X-Identification of Transition Delay Fault Tests for Launch-off Shift Scheme
Kohei Miyase, Fangmei Wu, Luigi Dilillo, Alberto Bosio, Patrick Girard, Xiaoqing Wen and Seiji Kajihara

S5-3 A Comprehensive Functional Time Expansion Model Generation Method for Datapaths

Using Controllers
Toshinori Hosokawa, Teppei Hayakawa and Masayoshi Yoshimura

S5-4 Functional Fault Model for Micro Operation Faults of High Correlation with Stuck-At Faults
Chia Yee Ooi and Hideo Fujiwara

Session 6: Other

Chair:

S6-1 A Scalable Test Access Mechanism for Godson-T Multi-core Processor
Luning Kong, Yu Hu and Xiaowei Li

S6-2 Low-Power DLL-based On-Product Clock Generation for 3D Integrated Circuit Testing
Michael Buttrick and Sandip Kundu

S6-3 Clock Signal Modulation for IC Electromagnetic Compatibility
Felipe Lavratti, Leticia Maria Bolzani Pöhls, Jorge Semião, Fabian Vargas, Juan Rodriguez-Andina, Isabel Teixeira and João Paulo Teixeira

S6-4 Design for Efficient Speed-Binning and Circuit Failure Prediction and Detection
Songwei Pei, Huawei Li and Xiaowei Li

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Venue

Convenient, Central Location. Four Points by Sheraton Shanghai, Daning is located north of Shanghai's central business district, Zha Bei – an area known for its infrastructure, cultural centers, universities, and multimedia industry. We're just a few minutes walk from the Yanchang Road subway station, close to Shanghai Circus World, and within easy access of the North-South Elevated Highway and Central Ring Road. Our hotel is also just three kilometers from the Shanghai Railway Station, 15 minutes from the People's Square, 25 minutes from Hongqiao Airport, and 45 minutes from Pudong International Airport.

Plenty to See & Do. As part of the new Life Hub @ DANING, an open-air lifestyle center, we are surrounded by offices, retail, restaurants, entertainment choices, culture, and education services. Plus, we have our own health club, heated indoor swimming pool, and spa.

Total Comfort & Spirited Service. 326 guest rooms and suites have it all - with a large LCD flat screen TV, jet shower, and the Four Points by Sheraton Four Comfort Bed. Plenty of meeting space, a business center, and wireless Internet in all meeting rooms and public areas keep the world at home at your fingertips.