WRTLT'11

IEEE Twelfth Workshop on RTL and High Level Testing 2011
MNIT Jaipur, India November 25-26, 2011

Workshop in Honour of Prof Fujiwara

The purpose of this workshop is to bring researchers and practitioners on VLSI testing from all over the world together to exchange ideas and experiences on register transfer level (RTL) and high level testing. The twelfth workshop on RTL and high level testing (WRTLT'11) will be held in conjunction with the 20th Asian Test Symposium (ATS'11). The workshop aims to encourage the presentation and discussion of truly innovative and "out-of-the-box" ideas aimed at addressing these challenges of high level test. We hope the workshop will provide an ideal forum for future complex system test at higher level of abstraction.

Representative topics include, but not limited to:

- Functional fault modeling
- Microprocessor testing
- Relationship between RTL and gate-level testing
- High level test bench generation
- High level approaches for testing
- RTL ATPG
- RTL BIST
- Design Verification
- SoC/NoC Testing
- Secure Testing
- 3D IC Test

Submission Details:
To present at the Workshop, authors are invited to submit previously unpublished technical proposals. The proposals must be full papers of maximum 8 pages or an extended summary. Each submission should include: title, full name and affiliation of all authors, a short abstract of 50 words, and keywords. Also, identify a contact author and include a complete correspondence address, phone number, fax number, and e-mail address.
Submit a copy of your proposal by PDF, via **easy chair** or via E-mail to : wrtlt2011@serc.iisc.ernet.in

Important Dates:

Paper Submission:	August 31, 2011 (Extended)
Author Notification:	September 25, 2011
Final Paper Submission:	October 15, 2011

Organizing Committee

General Co-Chairs
Rubin Parekhji (TI, IN)
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Preliminary Program (pdf)

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To Be Updated...

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VISA INFORMATION

WRTLT'11 has obtained the required political clearance from Ministry of External Affairs, India. If needed, you can attach a copy of this clearance along with your Visa application.

Also, the clearance from Ministry of Home Affairs, India, can be found here.

In general, non-Indian nationals require Visa to travel to India. Please contact the nearest Indian Embassy or Consulate in your country for Visa related details.

The Organizing Committee, WRTLT - 2011, will be very happy to send you an Invitation Letter required for obtaining your Visa. Please send us your passport details as given below, so that we can issue the Invitation Letter.

Title: Prof/Dr/Mr/Ms
Name: _____
(As on Passport)
Nationality: _____
Passport Number: _____
Place of Issue: _____
Date of Issue: _____
Passport valid till: _____
Affiliation: _____
Mailing Address: _____
Phone number: _____

Since the Visa process can take time, you are requested to send the above mentioned details to the General Chair (gaurms **at** gmail **dot** com) urgently, so that Letter of Invitation can be issued on priority basis.

If you need a Visa to visit India, please note the following:

A) Please send an email to the General Chair (gaurms **at** gmail **dot** com) with all the required information mentioned above. The local organizer will then issue you an invitation letter.

B) Please note that as WRTLT is a technical conference and the organizer MNIT Jaipur is a Government Educational Institution, no further clearance is required except for the citizens of Afghanistan, China, Iran, Pakistan, Iraq, Sudan, foreigners of Pakistani origin and Stateless persons. Please visit the following website for further details **FAQs on India Visa**.

More concretely, the following clearance documents are NOT required for conference Visa application:

1. A copy of event clearance from the Ministry of Home Affairs, Government of India (GoI).
2. Administrative approval of the Nodal Ministry, Government of India (GoI).
3. Political clearance from the M/O External Affairs, Government of India (GoI).
4. Clearance from the concerned State Government (s).

C) Please include this letter with your Visa application which clearly states that no clearance document is required.

D) If you are citizen of Afghanistan, China, Iran, Pakistan, Iraq, Sudan, foreigners of Pakistani origin and Stateless persons, we will provide you with the clearance documents.

E) If you face any difficulty with the Visa process, please get in touch with the General Chair Prof. MS Gaur (gaurms **at** gmail **dot** com) immediately so that the appropriate documents can be provided.

F) Please inform Prof. MS Gaur (gaurms **at** gmail **dot** com) once your Visa application is successful.

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Malaviya National Institute of Technology Jaipur
मालवीय राष्ट्रीय प्रौद्योगिकी संस्थान जयपुर

The Workshop will be held at Seminar Hall at Design Centre in MNIT, Jaipur

Please find detailed directions to reach MNIT Jaipur Here

Jaipur is situated in Northern India at a distance of around 260 km south-west of Delhi. It offers a multitude of interesting places and attractions. Such as lush parks and places for recreation. There are several magnificent palaces and forts. It is a city of fun, food and festivals. Vibrant colors, lively folk music and dance performances mark the celebrations of every religious occasion and every change of season.

How to reach Jaipur by air:

Information about Jaipur Airport

Information about Flight Schedule

Online Flight Booking:

Expedia

Make My Trip

How to reach MNIT from Sanganer Airport:

MNIT is roughly five kilometers from Sanganer Airport, from there one can either hire a prepaid taxi (Approximate charges are INR 250), or take a bus.

Bus Route: Take bus no 13 to reach Tonk Phatak —> Take bus no 7 (or 17) to reach MNIT.

How to reach Jaipur by Bus:

Jaipur is well connected by road network from Delhi, Agra, Udaipur, Jodhpur, etc. From Delhi: Volvo buses are available from Bikaner House on Pandhara Road (Near India Gate, New Delhi).

Bus Information (RSRTC)

How to reach Jaipur by Train:

Jaipur is well connected by train network from Delhi, Agra, Mumbai, Kolkata, Bangalore, Chennai, etc.

Train Information (Indian Railways)

Important Note: (For ATS Attendees)

Please note that transport facility would be arranged for ATS attendees from Delhi to Jaipur, via Agra (**Taj Mahal** Sightseeing) on request. Interested people, please write to local organizing chair <lavab **at** yahoo **dot** com>.

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All the room at "redfox Hotels" at the discounted rates have been booked.

Delegates can now opt for "Hotel Boutique"

S- 1O, Subhash Marg , C-Schme , Behind MGF Mall, Jaipur
Contact detail— 0141-2221048,2220988
(amit **at** rsmpholdings **dot** com)

Charges: 2,700 INR + Taxes (Including breakfast)

To avail these rates, please send an email to

raisondetre **dot** event **at** gmail **dot** com (Ph:+919649920390)
Prof MS Gaur (gaurms **at** gmail **dot** com)
With WRTLT 2011 BOOKING in the subject

redfox HOTELS

Other Hotels
Hotel Clarks Amer Jaipur
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WRTLT Registration:

Online Registration

The spot registration shall be done in Indian Currency (Rs.) only. Delegates opting for on the spot registration are requested to pay Rs. 12,500 either in cash or by cheque, in INR only.

Please write to **Jaynarayan Tudu** for more information about registration.
He can be reached at:

jaynarayan004 **at** gmail **dot** com
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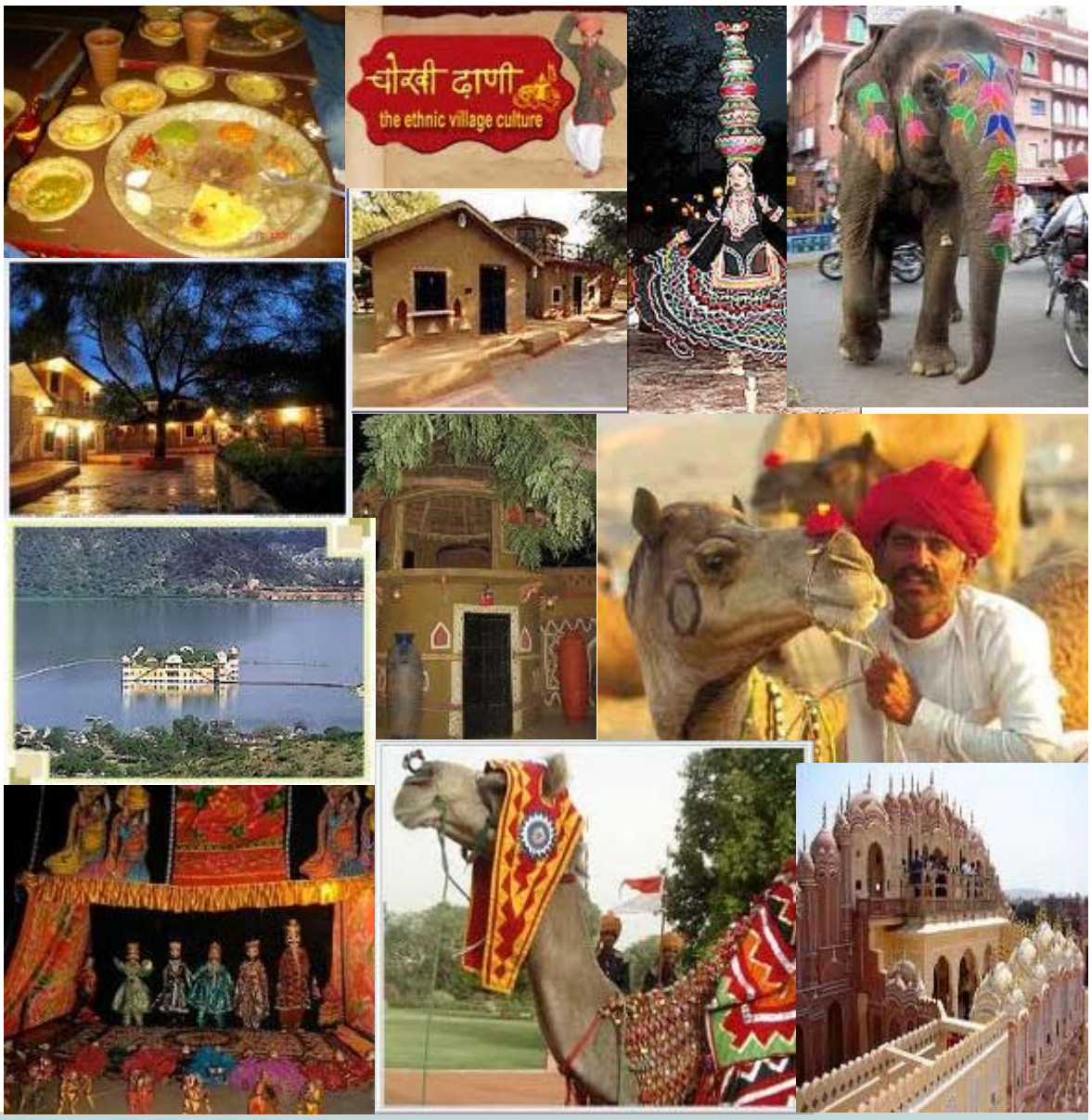




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Virendra Singh, IISc, Bangalore, India
Email: viren@serc.iisc.ernet.in

Preliminary Program- WRTLT2011

Day-1(Friday, 25th November)

Time	Event
8:30 to 9:00	Registration Coffee
9:00 to 9:15	Opening Ceremony
9:15 to 9:50	Keynote 1 Speaker: Masahiro Fujita Topic: Structural and Functional Test Generation from RTL/Behavioural Description
9:50 to 11:05	Session-1 *High Level Verification and Testing* *Session Chair: Zainalabedeen Navabi*
11:05 to 11:20	Tea Break
11:20 to 13:00	Session-2 *Delay Testing* *Session Chair: Chia Yee Ooi*
13:00 to 14:00	Lunch
14:00 to 19:00	Cultural Trip
19:00 to 21:00	Banquet
End of Day-1	

Day-2(Saturday, 26th November)

Time	Event
8:30 to 9:10	Keynote 2 Speaker: Hans-Joachim Wunderlich Mixed-level Techniques for Test, Validation and Evaluation of Digital Systems
9:10 to 10:25	Session-3 IEEE Standards 1149.1 & P1687, Compaction Session Chair: Joan Figueras
10:25 to 10:45	Tea Break
10:45 to 11:15	Invited Talk Speaker: Jaan Raik Topic: Applications of RTL Test Generation: Past, Present and Future
11:15 to 12:30	Session-4 *Secure & Dependable Design*

	Session chair: Ilia Polian
12:30 to 13:30	Lunch
13:30 to 14:45	Session-5 *Processor Testing, ATPG Acceleration* *Session Chair: Anzhela Matrosova*
14:45 to 14:50	Tea Break
15:05 to 16:20	Session-6 *Delay Measurement & Testing* *Session Chair:* Ioana Vatajelu
16:20 to 16:35	Tea Break
16:35 to 17:35	Panel Discussion Topic: Test Sign Off at RTL: Will it be a reality Moderator: Jaan Raik **Panelists:** Nilanjan Mukherjee Kazumi Hatayama Prab Varma Adit Singh
17:35 to 17:55	Vote of thanks
End of Day-2 and End of WRTLT-11	

Sessions

Session-1:

S-1.1 *Built-in Self-Test for Functional Register-Transfer Level using Assignment Decision Diagram,*

Norlina Paraman, Chia Yee Ooi, Ahmad Zuri Sha`ameri and Hideo Fujiwara

S-1.2 *A Binding Method for Hierarchical Testing Using Results of Test Environment Generation,*

Hiroaki Fujiwara, Toshinori Hosokawa, Ryoichi Inoue and Hideo Fujiwara

S-1.3 *Testability Challenges of Mixed-Signal SoC with Integrated Power Management: Unified Top Level Design, Verification and Test Methodology,*

Lakshmanan Balasubramanian and R. K. Mittal

Session-2

S-2.1 *Additional Path Delay Fault Detection with Adaptive Test Data,*

Kohei Miyase, Hiroaki Tanaka, Kazunari Enokimoto, Xiaoqing Wen and Seiji Kajihara

S-2.2 *On the Optimality of K Longest Path Generation,*

Jie Jiang, Matthias Sauer, Alexander Czutro, Bernd Becker and Ilia Polian

S-2.3 *Path Selection for High-Quality Small Delay Defect Testing,*

Dong Xiang

S-2.4 *Robust PDFs Testing of Combinational Circuits based on Covering BDDs,* Anzhela Matrosova, Ekaterina Nikolaeva, Sergey Ostanin and Virendra Singh

Session-3

S-3.1 *Extending BS-1149.1 for Interconnect Online BIST*,

Somayeh Sadeghi-Kohan, Ghazaleh Vazhbakht, Parisa Shaafi Kabiri and Zainalabedin Navabi

S-3.2 *A Study of Instrument Reuse and Retargeting in P1687,*

Farrokh Ghani Zadegan, Urban Ingelsson, Gunnar Carlsson and Erik Larsson

S-3.3 *A Test Compaction Oriented Don't Care Identification Method*,

Hiroshi Yamazaki, Motohiro Wakazono, Toshinori Hosokawa and Masayoshi Yoshimura

Session-4

S-4.1 *SR-Quasi-Equivalents: Yet Another Approach to Secure and Testable Scan Design,*

Katsuya Fujiwara, Hideo Fujiwara and Hideo Tamamoto

S-4.2 *Gracefully Degradable 3D On-Chip Networks Using an Optimized Rerouting Mechanism,*

Ali Shahabi, Reza Nakhjavani, Safari Saeed and Zainalabedin Navabi

S-4.3 *Self-Calibration using Functional BIST for Transient-Fault-Tolerant Sequential Circuits in Severe Electromagnetic Environment,*

Masayuki Arai, Aromhack Saysanasongkham, Kenta Imai, Yoshifumi Koyama

and Satoshi Fukumoto

Session-5

S-5.1 *On the Functional Test of Branch Prediction Units*,

Ernesto Sanchez and Matteo Sonza Reorda

S-5.2 *Hierarchical Instruction Level Self Testing of Embedded Processor Cores*,

Parisa Shaafi Kabiri and Zainalabedin Navabi

S-5.3 *Approach to Hardware SAT Solver for Test Generation Based on Instance Similarity,*

Tsuyoshi Iwagaki, Hideyuki Ichihara, Fumiyuki Hafuri, Kenji Ueda, Toshiya Mukai, Hideyuki Ichihara, and Tomoo Inoue

Session-6

S-6.1 *Reconfigurable Array-Based Area-Efficient Test Structure for Standard Cell Characterization*,

Bishnu Prasad Das and Hidetoshi Onodera

S-6.2 ESDQL: A *Metric for Evaluating Small Delay Defect Coverage*

Xuefeng Zhu and Huawei Li

S-6.3 Selection *of the Flip-Flops for Partial Enhanced Scan Techniques,*

Anzhela Matrosova, Alexey Melnikov, Ruslan Mukhamedov, and Sergey Ostanin

No. AA/161/01/2011-528
विदेश मंत्रालय / Ministry of External Affairs
समन्वय प्रभाग / Coordination Division
****

South Block, New Delhi
21st October, 2011

To

Malaviya National Institute of Technology,
Computer Engineering Department,
[Kind Attn: Dr. M.S.Gaur, General Program Chair],
Jaipur - 302017. (Fax: 0141-2529154)

Subject : Political Clearance for organizing "IEEE 12th Workshop on RTL and High Level Testing (WRTLT)" at Malaviya National Institute of Technology, Jaipur during 25-26 November, 2011.

Sir,

Please refer to your letter dated 5th August, 2011 on the above mentioned subject.

2. This Ministry has **No objection from Political angle,** for organizing of the proposed events, with participation of delegates from China and Iran, as per list attached, as stated in your aforesaid communication, subject to clearance of Home Affairs and other competent authorities.

Yours faithfully,

(R.K.Nagpal)
Deputy Secretary(Coord)

Copy to : Ministry of Home Affairs, [Kind Attn : Shri S.K.Singh, SO (CC)],
Foreigners Division, Jaisalmer House, 26 Mansingh Road, New Delhi.

F. N o. 4211857/CC
Ministry of Home Affairs
Foreigners Division
(Computer Cell)

Jaisalmer House,
26 Man Singh Road,
New Delhi- 110011,
dated 05.10.2011

OFFICE MEMORANDUM

Subject :- **IEEE 12TH workshop on RTL and high level testing, Nov.25-26, 2011 at Malaviya National Institute of Technology, Jaipur.**

The undersigned is directed to refer to your letter No. nil DT. 08.9.2011on the subject cited above and to say that this Ministry has 'no objection' in principle from the security angle for holding of the event(s) on the subject, dates and venue specified in the letter under reference subject to Political clearance by Ministry of External Affairs.

2. For authorization of visa to participants from (1) Afghanistan, (2) China, (3) Iran, (4) Iraq, (5) Pakistan, (6) Sudan, (7) foreigners of Pakistani Origin and (8) Stateless persons, the information (in the format given below) is required to be submitted to the Ministry of Home Affairs (Foreigners Division) at least 60 days before the commencement of the said event(s):

S.NO.	Name	Father's/ Husband's name	DOB	POB	Nationality & Ppt. No.	Date of issue	Place of issue	Date of Expiry	Address

3. It is also requested that participants from Pakistan may be advised to apply for visa at HCI, Islamabad 'on line' and the Unique ID (File No.) of the visa application may be intimated to this Ministry.

4. However, necessary action is being taken by this Ministry for grant of security clearance for authorization of visa to the following invitees, (as per list enclosed) whose personal particulars/ details in the prescribed format has already been submitted to this office.

5. So far as visa authorization to participants from the countries other than those as mentioned in para 2 above, Indian Mission abroad are authorized to issue conference visas to delegates on production of an invitation letter from the organizer(s).
In this context, FAQs on 'Conference Visa' uploaded under citizen services on MHA's website www.mha.nic.in. may be referred.

(S. K. Singh)
Section Officer

Dr. M.S. Gaur,
General Program Chair,
Professor, Computer Engg. Department,
Malaviya National Institute of Technology,
Jaipur.