Preliminary Program- WRTLT2011

Day-1(Friday, 25th November)

Time	Event
8:30 to 9:00	Registration Coffee
9:00 to 9:15	Opening Ceremony
9:15 to 9:50	Keynote 1 Speaker: Masahiro Fujita Topic: Structural and Functional Test Generation from RTL/Behavioural Description
9:50 to 11:05	Session-1 *High Level Verification and Testing* *Session Chair: Zainalabedeen Navabi*
11:05 to 11:20	Tea Break
11:20 to 13:00	Session-2 *Delay Testing* *Session Chair: Chia Yee Ooi*
13:00 to 14:00	Lunch
14:00 to 19:00	Cultural Trip
19:00 to 21:00	Banquet
End of Day-1	

Day-2(Saturday, 26th November)

Time	Event
8:30 to 9:10	Keynote 2 Speaker: Hans-Joachim Wunderlich Mixed-level Techniques for Test, Validation and Evaluation of Digital Systems
9:10 to 10:25	Session-3 IEEE Standards 1149.1 & P1687, Compaction Session Chair: Joan Figueras
10:25 to 10:45	Tea Break
10:45 to 11:15	Invited Talk Speaker: Jaan Raik Topic: Applications of RTL Test Generation: Past, Present and Future
11:15 to 12:30	Session-4 *Secure & Dependable Design*

	Session chair: Ilia Polian
12:30 to 13:30	Lunch
13:30 to 14:45	Session-5 *Processor Testing, ATPG Acceleration* *Session Chair: Anzhela Matrosova*
14:45 to 14:50	Tea Break
15:05 to 16:20	Session-6 *Delay Measurement & Testing* *Session Chair:* Ioana Vatajelu
16:20 to 16:35	Tea Break
16:35 to 17:35	Panel Discussion Topic: Test Sign Off at RTL: Will it be a reality Moderator: Jaan Raik **Panelists:** Nilanjan Mukherjee Kazumi Hatayama Prab Varma Adit Singh
17:35 to 17:55	Vote of thanks
End of Day-2 and End of WRTLT-11	

Sessions

Session-1:

S-1.1 *Built-in Self-Test for Functional Register-Transfer Level using Assignment Decision Diagram,*

Norlina Paraman, Chia Yee Ooi, Ahmad Zuri Sha`ameri and Hideo Fujiwara

S-1.2 *A Binding Method for Hierarchical Testing Using Results of Test Environment Generation,*

Hiroaki Fujiwara, Toshinori Hosokawa, Ryoichi Inoue and Hideo Fujiwara

S-1.3 *Testability Challenges of Mixed-Signal SoC with Integrated Power Management: Unified Top Level Design, Verification and Test Methodology,*

Lakshmanan Balasubramanian and R. K. Mittal

Session-2

S-2.1 *Additional Path Delay Fault Detection with Adaptive Test Data,*

Kohei Miyase, Hiroaki Tanaka, Kazunari Enokimoto, Xiaoqing Wen and Seiji Kajihara

S-2.2 *On the Optimality of K Longest Path Generation,*

Jie Jiang, Matthias Sauer, Alexander Czutro, Bernd Becker and Ilia Polian

S-2.3 *Path Selection for High-Quality Small Delay Defect Testing,*

Dong Xiang

S-2.4 *Robust PDFs Testing of Combinational Circuits based on Covering BDDs,* Anzhela Matrosova, Ekaterina Nikolaeva, Sergey Ostanin and Virendra Singh

Session-3

S-3.1 *Extending BS-1149.1 for Interconnect Online BIST*,

Somayeh Sadeghi-Kohan, Ghazaleh Vazhbakht, Parisa Shaafi Kabiri and Zainalabedin Navabi

S-3.2 *A Study of Instrument Reuse and Retargeting in P1687,*

Farrokh Ghani Zadegan, Urban Ingelsson, Gunnar Carlsson and Erik Larsson

S-3.3 *A Test Compaction Oriented Don't Care Identification Method*,

Hiroshi Yamazaki, Motohiro Wakazono, Toshinori Hosokawa and Masayoshi Yoshimura

Session-4

S-4.1 *SR-Quasi-Equivalents: Yet Another Approach to Secure and Testable Scan Design,*

Katsuya Fujiwara, Hideo Fujiwara and Hideo Tamamoto

S-4.2 *Gracefully Degradable 3D On-Chip Networks Using an Optimized Rerouting Mechanism,*

Ali Shahabi, Reza Nakhjavani, Safari Saeed and Zainalabedin Navabi

S-4.3 *Self-Calibration using Functional BIST for Transient-Fault-Tolerant Sequential Circuits in Severe Electromagnetic Environment,*

Masayuki Arai, Aromhack Saysanasongkham, Kenta Imai, Yoshifumi Koyama

and Satoshi Fukumoto

Session-5

S-5.1 *On the Functional Test of Branch Prediction Units*,

Ernesto Sanchez and Matteo Sonza Reorda

S-5.2 *Hierarchical Instruction Level Self Testing of Embedded Processor Cores*,

Parisa Shaafi Kabiri and Zainalabedin Navabi

S-5.3 *Approach to Hardware SAT Solver for Test Generation Based on Instance Similarity,*

Tsuyoshi Iwagaki, Hideyuki Ichihara, Fumiyuki Hafuri, Kenji Ueda, Toshiya Mukai, Hideyuki Ichihara, and Tomoo Inoue

Session-6

S-6.1 *Reconfigurable Array-Based Area-Efficient Test Structure for Standard Cell Characterization*,

Bishnu Prasad Das and Hidetoshi Onodera

S-6.2 ESDQL: A *Metric for Evaluating Small Delay Defect Coverage*

Xuefeng Zhu and Huawei Li

S-6.3 Selection *of the Flip-Flops for Partial Enhanced Scan Techniques,*

Anzhela Matrosova, Alexey Melnikov, Ruslan Mukhamedov, and Sergey Ostanin