WRTLT'12 Final Program

Nov. 22-23, 2012, Toki Messe Niigata Convention Center, Niigata, Japan

November 22, 2012

11:30 –Registration

12:00 – 13:15 Welcome lunch (Gekka Hyojin (2F))

13:25 – 13:35 Opening

13:35 – 14:35 Plenary Session 1

Session Chair: T. Inoue (Hiroshima City University)

Keynote Address

Hardware Trojans: Threats and Emerging Solutions
R. S. Chakraborty (Indian Institute of Technology, Kharagpur)

Invited Talk (1)

TRUDEVICE: a COST Action in Europe
I. Polian (University of Passau)

14:35 – 14:40 Break

14:40 – 15:30 Session 1 High Level Testing & Secure Testing

Session Chair: E. Larsson (Lund University)

1.1 Generating Directed Tests for C Programs using RTL ATPG
T. Drenkhan, A. Tšepurov, T. Viilukas, J. Raik, A. Karputkin, M. Jenihhin, R. Ubar (Tallinn University of Technology)
1.2 WAGSR: Web Application for Generalized Feed Forward Shift Registers
K. Fujiwara (Akita University), H. Fujiwara (Osaka Gakuin University)
1.3 An Estimation of Trojan Circuits on AES Encryption Circuits
M. Yoshimura (Kyushu University), A. Ogita, T. Hosokawa (Nihon University)

15:30 – 15:45 Break

15:45 – 17:05 Session 2 Test Generation & Design for Testability

Session Chair: S. Ohtake (Oita University)

2.1 On detectability analysis of open faults using SAT-based test pattern generation considering adjacent lines
J. Yamashita, H. Yotsuyanagi, M. Hashizume (University of Tokushima), K. Kinoshita (Osaka Gakuin University)
2.2 Towards Increasing Test Compaction Abilities of SAT-based ATPG through Fault Detection Constraints
S. Eggersglüß (DFKI/ University of Bremen), M. Diepenbeck, R. Wille (University of Bremen), R. Drechsler (DFKI)
2.3 Estimating the Number of Don't-Care Bits in Test Vectors
K. Miyase, S. Kajihara, X. Wen (Kyushu Institute of Technology)
2.4 A Test Point Insertion Method Using Don’t Care Identification and Test Compaction Techniques to Reduce Test Application Time for Transition Faults
T. Hosokawa, A. Takahashi, H. Yamazaki (Nihon University), M. Yoshimura (Kyushu University)

17:05 – 17:10 Break

17:10 – 18:05 Session 3 Reliability & Dependable SoC
Session Chair: H. Yotsuyanagi (University of Tokushima)

3.1 Which Metric is Better for Quantification of Hardware Faults-induced Errors?
Y. Fang, H. Li, X. Li (Chinese Academy of Sciences)
3.2 A Realization Method of Fast and Dependable Programmable Logic Controllers
R. Kawaguchi, Y. Yamada, K. Takahashi, Y. Urano, Y. Iguchi (Meiji University)
3.3 A Study on Error Correctable Test Pattern Generator for Reliable Built-in Self Test
Y. Fukazawa, T. Iwagaki, H. Ichihara, T. Inoue (Hiroshima City University)

18:05 – 18:30 Break

18:30 – 20:30 Banquet (Hotel Nikko Niigata, Sky Banquet Tsuru(30F))

November 23, 2012

8:30 –Registration

9:00 – 10:10 Plenary Session 2
Session Chair: X. Li (Chinese Academy of Sciences)
Invited Talk (2)

The Past and Future of WRTLT
Y. Min (Chinese Academy of Sciences), H. Fujiwara (Osaka Gakuin University)

Invited Talk (3)

System Level Testing Considerations as we Move from RTL to ESL
Z. Navabi (University of Tehran)

10:10 – 10:25 Break

10:25 – 11:40 Session 4 Delay Testing
Session Chair: H. Takahashi (Ehime University)

4.1 Capturing Post-Silicon Variations by Layout-Aware Path-Delay Testing
X. Zhang, J. Ye, Y. Hu, X. Li, H. Li (Chinese Academy of Science)
4.2 Exact and Heuristic Methods of Generating Compact Tests for Hold-time Violations
T. Iwagaki, H. Ichihara, T. Inoue (Hiroshima City University), K. K. Saluja (University of Wisconsin-Madison)
4.3 A Reduction Technique of Volume of Input Sequences for Time-Multiplexed Delay Measurement Using Embedded Delay Measurement Circuit
K. Katoh, S. Hoshina (Tsuruoka National College of Technology), K. Itagaki (Nagaoka University of Technology)
4.4 Delay measurement of global routing resources in FPGA for small delay defect detection
K. Namba, N. Takashina, H. Ito (Chiba University)

11:40 – 13:10 Lunch

13:10 – 14:20 Panel Session

Theme: "Can RTL test techniques be applied to software?"
Coordinator: J. Raik (Tallinn University of Technology)
Panelists:
G. Fey (Bremen University/ German Institute for Aerospace DLR)
M. Fujita (University of Tokyo)
Z. Navabi (University of Tehran/ Worcester Polytechnic Institute)
H. Li (Chinese Academy of Sciences)

14:20 – 14:35 Break

14:35 – 15:50 Session 5 Low Power Testing & Online Testing

Session Chair: J.-L. Huang (National Taiwan University)

5.1 An Efficient Fault Simulation Algorithm for Analyzing Incorrect State Transitions Induced by Soft Errors in Sequential Circuits
T. Takata, M. Yoshimura, Y. Matsunaga (Kyushu University)
5.2 Power Aware Scan Flip Flop Design for Scan Test
S. Ahlawat (Indian Institute of Technology, Bombay), J. T. Tudu (Indian Institute of Science, Bangalore), A. K. Suhag (Gautam Buddha University), V. Singh (Indian Institute of Technology, Bombay)
5.3 An Improved Method of Per-Cell Dynamic IR-Drop Estimation Based on the Weighted Switching Activity Metric
Y. Yamato, Y. Akiyoshi, T. Yoneda, K. Hatayama, M. Inoue (NAIST)
5.4 An Online Method for Serial Interconnects Testing
S. S.-Kohan, S. Keshavarz, Z. Navabi (University of Tehran)

15:50 – 16:05 Break

16:05 – 16:55 Session 6 NoC Testing & 3D IC Testing

Session Chair: T. Yoneda (Nara Institute of Science and Technology)

6.1 Output Voltage Estimation Method of Hard Open TSV in 3D ICs
M. Hashizume, S. Kondo, E. Haraguchi, H. Yotsuyanagi (University of Tokushima), T. Tada (Tokushima Bunri University), Z. Roth (Florida Atlantic University)
6.2 A Cost-Effective Scheme for 3-D Stacked Network-on-Chip Router and Interconnect Testing
D. Xiang, G. Liu (Tsinghua University)
6.3 An Algorithm for Core-Based Test Time Optimization for 3-D Integrated Circuits
M. Pradhan (Jadavpur University), C. Giri, H. Rahaman (Bengal Engineering and Science University, Shibpur) , D. K. Das (Jadavpur University)

16:55 – 17:00 Closing

WRTLT2012 Accommodation

Welcome Lunch:
    Nov. 22, 12:00-13:15 Gekka Hyojin(2F)
Banquet
    Nov. 22, 18:30-20:30 Tsuru, Hotel Nikko Niigata(30F)